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Printed circuit board technologies updated for intelligent power systems – page 10

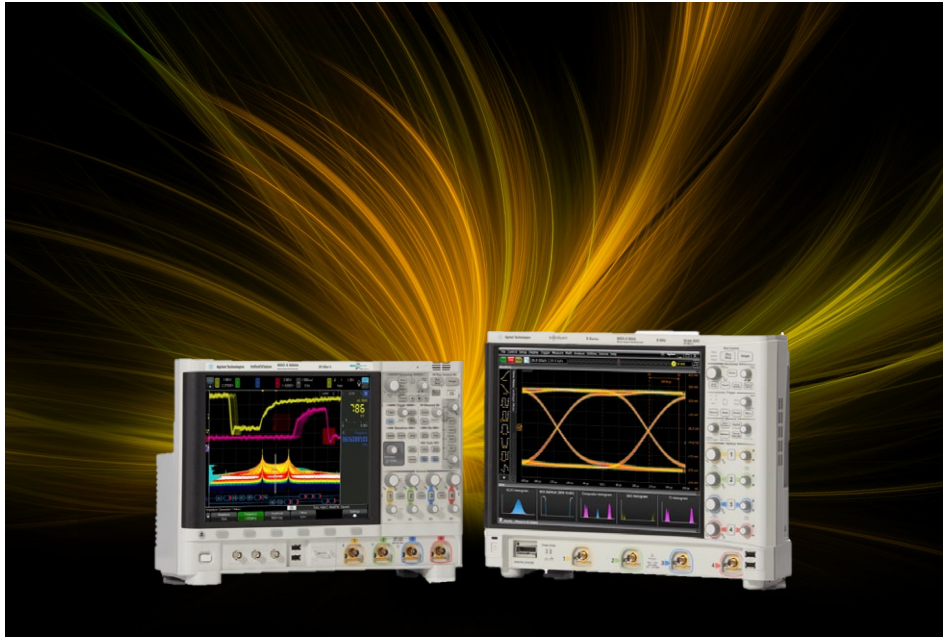
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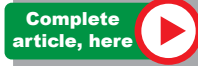
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Size trends in medical sensing; compact technology meets patient needs – page 26



Cover Image

The cover image is by Agilent Technologies which has introduced two high-performance, large-screen capacitive-touch-controlled portable oscilloscope series; the Infiniium S-Series focuses on signal integrity for bandwidths up to 8 GHz, while the InfiniiVision 6000 X-Series offers higher price/performance with bandwidths up to 6 GHz, and introduces voice control of basic functions.



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IOT HITS THE RISK RADAR

I am indebted to Juerg Siegenthaler of Avnet Memec – which company has recently made an announcement around placing increased resources into servicing the development of connected-devices – for bringing to my attention an announcement from the Zurich Insurance Group. The insurer has recently issued a *Cyber Risk Report*, in which it identifies seven major categories of risk to the global economy in general, and to companies, organisations, and countries, of untoward happenings in cyberspace – whether these be maliciously-invoked, caused by natural phenomena, or an inadvertent consequence of our use of the IT space, or arising spontaneously from the complexity we have created.

Of particular note for designers in the embedded systems space is that already – some might say, none too soon – the insurer already identifies the Internet of Things as a potential hazard. Before getting to that point, the report reflects on the similarities between the unappreciated instabilities of global financial markets that led to the 2008 ‘meltdown’ and the hidden complexities of the Internet and its associated systems. “Sub-prime” investments were bought, sold, divided, parcelled up, re-packaged and re-sold across the financial system, until no-one knew how much poor-quality debt was in the system, or where the liabilities really were. In a similar (at some level, at least) the Internet has grown piecemeal, and is extensively cross-connected, with an unknown – and, perhaps, unknowable – number of dependencies.

The report acknowledges the contribution of a myriad of programmers and engineers who daily patch and repair emerging flaws and “keep the show on the road” - it alludes to, although it does not use the term, the “Swiss Cheese” model of causes of disasters. That is to say, an Emmental naturally has holes within it; individual systems failures are equated to holes; any single failure or even limited number of concurrent failures are within the capability of the system to recover. If, however, one day all the holes were to line up, you could see all the way through – and that is when a disaster occurs. The Internet, and our dependence on it, has all the characteristics of vulnerability to a failure after which we would say, “we knew about the individual issues: but no-one anticipated that a particular sequence of events would concatenate with catastrophic results.”

Anyone involved in safety-critical systems design will identify with many of the points that the report makes; for example, about the problems of interdependence and “hyperconnectivity”. To quote, *“In cybersecurity a similar process occurs when companies outsource functions or information, allowing them to focus on core competencies, freeing them from the worries associated with managing servers, IT processes and security. All too often these companies know nothing of the information security or business continuity measures of the company to which they’ve outsourced. Worse, portions of the outsourced work often get further outsourced as each individual company focuses on its core competencies, and so on. Alternatively, a company might seek to mitigate risk by diversifying its outsourcing by, for example, working with four separate providers, only to find that in turn, they all rely on the same cloud service provider, on the*

same operating system, or on the same internet service providers.”

Accordingly, the Report identifies seven “Aggregations of cyber risk,” of which one is “Disruptive technologies.” Which it outlines as, “Risks from unseen effects of or disruptions either to or from new technologies, either those already existing but poorly understood, or those due soon.” And one of those is the Internet of Things; other examples used are embedded medical devices; driverless cars; and the largely automatic digital economy. This last is perhaps particularly frightening when viewed from an engineering perspective at even the most superficial level. “Algorithmic” trading now dominates activity in the major Western stock markets such as the New York Stock Exchange, leading to the situation that, as one interviewee in Forbes magazine put it, “All this noise comes from [market players] trying to game each other or fool traders.” Any control systems engineer will look at such a poorly-characterised configuration of competing algorithms and say, “Instability. Oscillation.” (Of course, the financial authorities know this, and try to guard against it, but the potential for unpredictable behaviour is implicit.)

The Zurich report notes that disruptive technologies, “generally include the range of innovations that increase our dependence in radical ways. The World Economic Forum calls this hyper-connectivity which “does not just allow us to do things more efficiently; it transforms how we do things and even what can be done.”

“The goals and implications are staggering, as “the internet now connects anywhere from 10 billion to 15 billion devices. Even so, less than one percent of things are connected to the internet today...”

When applied to the electrical grid, these technologies are referred to as the smart grid, a catch-all term for technologies “to bring utility electricity delivery systems into the 21st century, using computer-based remote control and automation.”

“Internet shocks could ripple through systems in countless ways, because of the universe of unknown and unknowable dependencies. As systems get more complex and interdependent, more tightly coupled and with fewer workarounds, the shocks from these systems will have an impact on, and echo in the ‘normal’ internet.”

An entirely reasonable response from the embedded-systems design community would be, “we knew that.” Nevertheless, it does no harm to realise that the other interested parties are also alert to the risks inherent in what we are creating. It is a safe, if unsettling, prediction that there will be major shocks to, and in, the system: and there will be allocations of blame, and potentially even searches for scapegoats. The wider world is already watching – also entirely reasonably, in the case of the insurers, as they will end up paying the bills – even before the IoT gets fully into its stride. As the paragraphs above confirm, it is in the nature of things that shocks will come “out of the blue”: but in any after-the-event analysis, being judged to have failed to anticipate something that could have been foreseen, will not be a comfortable place to be.



Agilent Technologies

Agilent's Electronic
Measurement Group



**Keysight
Technologies**

Agilent's Electronic Measurement Group,
including its 9,500 employees and 12,000
products, is becoming **Keysight Technologies**.

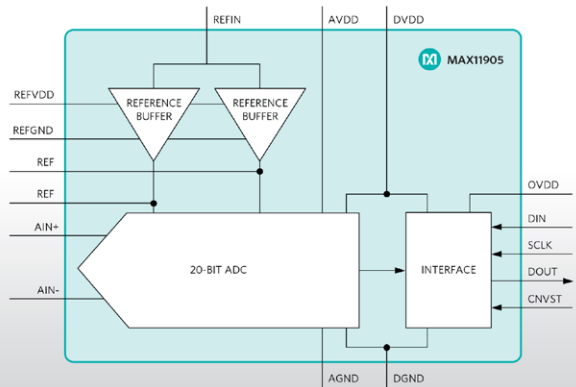
Learn more at www.keysight.com

pulse

20-bit SAR ADC wins on precision, speed, & power

Engineers can achieve the industry’s highest resolution and fastest sampling rate at the lowest power with the MAX11905, a 20-bit, 1.6 Msamples/sec successive approximation register (SAR) analogue-to-digital converter (ADC), while saving up to 91% power and up to 50% space. Typically, Maxim says, when you need high-precision data conversion, you may turn to a delta-sigma ADC. However, to produce high precision and wide dynamic range, those ADCs must consume at least 100 mW of power. The MAX11905 SAR ADC consumes 9 mW – a 91% power savings. With this power savings comes very high (20-bit) precision and the fastest sampling (1.6 Msamples/sec) rate available. The MAX11905 also integrates internal reference buffers, and saves up to 50% space compared to competitive discrete solutions. Use MAX11905 in applications including process control, automatic test equipment, medical instrumentation, and battery-powered devices. MAX11905 enables 1.6 Msamples/sec throughout with no latency and settling time limitation. The ADC achieves 98.3 dB signal-to-noise ratio (SNR) and -123 dB THD; improves static

Highly Integrated 20-Bit, 1.6Msps SAR ADC
MAX11905



and dynamic performance; guarantees monotonic function; and provides lowest power consumption. It delivers 20-bit resolution with no missing codes, at 1.6 Msamples/sec, and at 9mW. In a 20-pin, 4 x 4 mm TQFN package, and specified over -40 to +85C, it costs \$33.95 (1000).



ARM switches to open-source base for compiler updates

ARM has announced version 6 of the ARM Compiler, the reference code generation toolchain for the ARM architecture. Version 6 marks a shift from a fully-proprietary tool chain to one that is based on open-source code. ARM says that the “velocity” of open source Clang and LLVM, combined with the stability of commercial products, will improve code quality, performance and power efficiency on ARM processors. The company emphasises that the rest of the tool chain remains ARM-proprietary – the change is limited to the compiler and the distinction is that the compiler is “based on” open-source but is not in its entirety open-source. The first architecture to be supported under this arrangement will be ARM v8, for which ARM anticipates seeing the first silicon [at licensees] “soon”. This means that users will be able to draw on the open-source LLVM community for immediate improvements, and that ARM will



periodically – around twice a year – take a “snapshot” of the evolving code base, test and verify it, and give it a release number. The licensing context is also favourable to this approach, ARM says; being “permissive” it allows users to draw on the code base without necessarily feeding back their changes, so “closed”, tuned, versions are possible. Support for the established ARM compiler will continue in parallel, for, “anyone who wants or needs it,” the company says, citing in particular, users working on safety-critical systems. There will also continue to be a path for users developing for Linux/Android targets. ARM Compiler 6 supports the ARM Cortex-A50 processor series and is available as part of the DS-5 Development Studio Ultimate Edition, available now.



Altera drops “hard” floating point blocks into FPGAs

Altera is claiming a programmable-logic “first” with an announcement that it has implemented IEEE 754-compliant hardened floating-point DSP blocks on FPGAs, and that it is shipping the feature now, in its Arria 10 FPGAs. Among other advantages, designs can be finalised with floating-point DSP without the need to convert to fixed-point.

Integrating hardened IEEE 754-compliant, floating-point operators in an FPGA provides you with, Altera says, greater levels of DSP performance, designer productivity and logic efficiency. The hardened floating point DSP blocks are integrated in Altera’s 20 nm Arria 10 FPGAs and SoCs – currently shipping – and will be in its 14 nm Stratix 10 FPGAs and SoCs. Integrated hardened floating-point DSP blocks, combined with an advanced high-level tool flow, assist you to use Altera’s FPGAs and SoCs in computationally intensive applications, such as high-performance computing (HPC), radar, scientific and medical imaging.

The hardened single-precision floating point DSP blocks included in Arria 10 and Stratix 10 devices are based on Altera’s variable precision DSP architecture. Unlike traditional approaches that implement floating point by using fixed point multipliers and FPGA logic, Altera uses efficient, hardened floating point DSP blocks to eliminate nearly all the logic usage required for existing FPGA floating-point computations. This yields up to 1.5 TeraFLOPs (floating point operations per second) DSP performance in Arria 10 devices and up to 10 TeraFLOPs DSP performance in Stratix 10 devices, the company asserts. DSP designers are able to choose either fixed or floating-point modes and the floating point blocks are backwards compatible with existing designs.

FPGAs feature a fine-grained, highly pipelined architecture that make them ideally suited for use as high-performance compute accelerators. The inclusion of hardened floating-point DSP blocks enables designers to use Altera FPGAs to address more complex HPC problems in big data analytics, seismic modelling for oil and gas industries and financial simulations. Across these and other computationally intensive applications, FPGAs deliver the highest performance per Watt when compared to DSPs, CPUs and GPUs, Altera adds.

Altera further claims that you can also cut development time by months. Designers can translate their DSP designs directly into floating-point hardware, rather than converting their designs to fixed point. As a result, timing closure and verification times

are reduced. Altera also provides multiple tool flows that allow hardware designers, model-based designers and software programmers to target the high-performance floating-point DSP blocks in its devices.



Altera has also disclosed (story here) early results with the Intel 14-nm TriGate process; test chips it has fabricated in 14 nm finfet – or Tri-Gate, as Intel terms it – confirm expected performance, power and density advantages. Altera built some of its key intellectual property (IP) components – transceivers, mixed-signal IP and digital logic – used in Stratix 10 FPGAs and SoCs, on the test chips: Altera and Intel collaborated on the development of the industry’s first FPGA-based devices exploiting Intel’s process technology and Altera’s programmable logic technology.

Intel says it has a “true die shrink” with its second-generation 14 nm Tri-Gate process, relative to alternative FinFET technologies. In Intel’s 14 nm Tri-Gate process and an enhanced high-performance core fabric architecture, Stratix 10 FPGAs and SoCs will target advanced, high performance applications in the communications, military, broadcast and compute and storage markets, while cutting system power. Core operating performance will be up to 1 GHz. For high-performance systems that have the most strict power budgets, Stratix 10 devices allow customers to achieve up to a 70% reduction in power consumption by trading performance for power.

Complete article, [here](#)



Write “Cooler GUIs” with development editor

Altia is a user interface development software company that provides tools for the creation of graphical user interfaces for embedded devices, with users in automotive, medical, industrial, fitness, and home appliance industries. The latest release, Altia Design 11.1, is the centrepiece of Altia’s user interface development tool suite. With the new features

rolled into Altia Design 11.1, users are equipped to develop better GUIs than ever before, its writers claim.

Altia offers a GUI editor and graphics code generator that enable development teams to build completely custom user interface models with graphics created from scratch or imported from industry-standard design programs such as Adobe Photoshop. The Altia GUI can be connected to a variety of simulation tools or C code to create a complex, user-driven model which can be shared with users and management teams for testing and validation prior to production. Once approved, Altia’s code generator automatically generates pure C source



code that is optimised to take full advantage of the resources of the selected production hardware.

New features in Altia Design 11.1 include Validator that gives users the capability to perform real-time validation of their GUI design against general guidelines or even design rules specific to their selected embedded target. Users can now look “under the hood” while their GUI runs within Altia Design to review and trap animation activity with the new Debugger. The next generation of the Altia Design Display Object – the new Layer Manager – helps users to manage multi-layer designs, create screens and handle layer composition.

With Altia Design 11.1, users also can import and control eye-catching 3D mesh files and animations from 3D authoring tools. The Multi-Plot Object offers “cool” complex plotting, strip-charting and data logging capabilities for advanced applications such as medical and industrial user interfaces.



Dual-protocol module supports ANT and Bluetooth

Dynastream Innovation’s N548 module is aimed at Internet-of-things applications. Based on Nordic Semiconductor’s nRF51422 SoC, this 2.4 GHz solution is small and features concurrent support for both ANT and Bluetooth low energy.

The N548 is sized for wearable, home and industrial trends in a 14.0 x 9.8 x 2.0 mm LGA (Land Grid Array) package. Its makers say that it is a combination of technologies not previously available, taking ultra low power wireless to a new level of connectivity, and that, “ANT is always focused on simplifying issues for developers and this module offers all of the latest ANT and ANT+ advantages in a turnkey hardware solution.”



Designed for manufacturing simplicity, the N548 ANT SoC Module is fully integrated with PCB antenna, 32 kHz crystal time base, DC-DC converter, and 24 GPIOs with six analogue inputs, allowing developers the freedom to focus on their specific applications. It is pre-certified with FCC/IC/CE/JP/AU/NZ designations and Bluetooth qualification. Use it in simple sensors as well as cost-focused applications. The N548 highlights the advantages of the ANT protocol, including its strong position in

Android smart phones, while enabling a bridge connection between available ANT+ devices and the iOS platform.



French consortium formed to advance pedestrian inertial navigation systems

by Peter Clarke

Movea SA, developer of embedded software for sensor fusion and motion processing, is teaming up with MEMS foundry Tronics Microsystems SA and the Leti and List research institutes in Grenoble to develop an inertial measurement unit to allow pedestrian dead reckoning when geo-location by satellite is not available. The fourth member of the collaboration, and the only one not based in Grenoble, is aerospace and military consultancy EASII IC.

The project plans to produce a wearable device that includes sensors, processor, and data fusion algorithms that connects to a smartphone via Bluetooth.

Movea said the team plans to spend \$8.5 million over three years on the ASIMUT project to develop a module that makes it possible to measure the location and movements of people inside buildings and in other areas where global positioning by satellite (GPS) is not available. ASIMUT stands for Advanced

and Smart Inertial Measurement Unit. Current dead-reckoning systems, based on inertial sensors for step counting and a pressure sensor for estimating vertical movement, are known to lose accuracy when used for prolonged periods, as errors accumulate.

Applications for the technology include tracking activities such as lone worker safety inside a building or tracking firefighters, police and security workers during an emergency situation. The platform will also enable more commercial applications such as augmented reality displays for use in museums and shopping malls, Movea said. Movea will provide the software for the module and Tronics will provide the MEMS accelerometers and gyroscopes. EASII IC will build the industrial prototypes of the wearable device.

First demonstrations are expected in the middle of 2015.

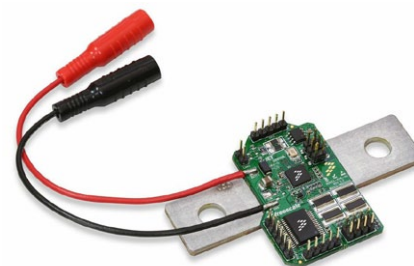


Battery sensor integrates MCU, CAN and analogue front-end

Freescale has an AEC-Q100 (automotive) qualified intelligent battery sensor that combines three measurement channels, a 16/32-bit MCU, and a CAN protocol module in a single package. Designed to support both conventional and emerging battery chemistries for automotive and industrial applications, the MM9Z1J638 battery sensor measures key battery parameters for monitoring state of health (SOH), state of charge (SOC) and state of function (SOF) for early failure prediction. A flexible four-cell front end architecture supports conventional 12V lead acid batteries as well as emerging battery applications, such as 14V stacked cell Li-Ion, high voltage junction boxes, and 24V truck batteries.

Integrating a 16/32 bit S12Z microcontroller with 128 k Flash, 8k RAM and 4k EEPROM together with a CAN protocol module, LIN interface and a three-channel analogue measurement

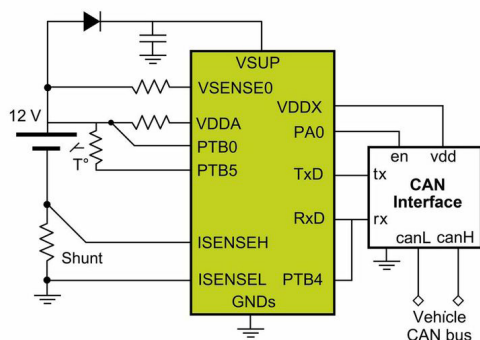
front end, the MM9Z1J638 battery sensor combines analogue, processor and communication functions in a single package to help lower total bill of materials and accommodate advanced battery monitoring algorithms. The analogue front end includes a two-channel, 16-bit sigma delta ($\Sigma\Delta$) analogue-to-digital converter (ADC) for simultaneous measurement of battery voltage and current, as well as a third 16-bit $\Sigma\Delta$ ADC for temperature monitoring using the integrated sensor and redundant measurement plausibility checks to support functional safety.



The new Freescale product's input battery voltage measurement capability supports a wide range up to 52V directly to the device as well as much higher voltage battery configurations when used with external voltage dividers.

Reference designs with integrated hardware and software support for the MM9Z1J638 battery sensor enable development of new applications, including energy storage systems, uninterruptible power supplies, hospital equipment and alarm systems. Low-level drivers and BMS utility libraries are available to support custom battery modelling and shorten development cycles. The KIT9Z1J638EVM evaluation board is priced at \$188.80 and demonstrates key features of the MM9Z1J638. Reference design RD9Z1-638-4Li is priced at \$220.80 and demonstrates product capabilities for 4-cell Li-Ion battery applications. The MM9Z1J638 battery sensor costs \$3.61(10,000).

MM9Z1_638 Simplified Application Drawing



12 V Application, CAN Communication



SERDES-centric 85k LUT FPGAs for companion-chip roles

A device family from Lattice, the ECP5, is intended for small-cell, microserver, broadband access, industrial video and other high-volume applications where the lowest-possible cost, lowest-possible-power, and smallest-possible form-factor are crucial. The ECP5 Family 'breaks the rules' of conventional FPGA approaches to deliver a SERDES-based solution for designers to rapidly add features and functions to complement those delivered by ASICs and ASSPs.

Lattice optimised the ECP5 family's architecture with the goal of delivering the best value below 100k LUTs for performing critical functions as a companion chip to ASICs and ASSPs. Achieving 40% lower cost than competing solutions, optimisations include small LUT4 based logic slices with enhanced routing architecture, dual-channel SERDES to save silicon real estate, and enhanced DSP blocks for up to 4x resource improvements. "The ECP5 family breaks the rule that FPGAs should be the highest density, power hungry and expensive," said Lattice Semiconductor President and CEO Darin Billerbeck. "Lattice's newest family serves to provide customers with an ASIC/ASSP companion chip as the quickest path for removing development

obstacles."

In wireless and wireline applications, the ECP5 family delivers an FPGA solution for enabling implementation of data path bridging and interfacing in a small, low-cost package. ECP5 FPGAs provide the flexible connectivity required in outdoor small-cells, at extremely low-cost. They can also enable a smart SFP (small form-factor pluggable) transceiver solution for broadband access equipment, including integrated operation and maintenance, in a 10m x 10mm package. Outside of communications, ECP5 devices offer low cost, low power PCI Express side-band connectivity for microservers. For industrial video cameras, ECP5 FPGAs can implement the entire image processing functionality in a device that consumes under 2W.

The ECP5 family is, says Lattice, the only FPGA portfolio that enables 85k LUTs and SERDES in 10 x 10mm packages, amounting to 2X the functional density of competing solutions. Smart ball depopulation further simplifies package integration with existing PCB technology and reducing overall system cost.



PRINTED CIRCUIT BOARD TECHNOLOGIES UPDATED FOR INTELLIGENT POWER SYSTEMS

Migration of electric power generation to the periphery of the grid is presenting new challenges for load balancing and synchronisation. The continuing need for greater efficiency in electric power utilisation and control also means that control systems are in the process of migrating towards individual loads. As a result, greater intelligence is required throughout the grid, from point of power generation to point of power consumption. And the combination of power and intelligence is presenting both challenges and opportunities to the electronics designer: challenges because small, cost-effective intelligent power management modules need to combine digital logic with mains power, and opportunity because new and innovative board level technologies exist to match this challenge.

The Problem

AC power management involves three basic functions; current sensing / measurement, phase detection / synchronisation, and switching. The classic electric power meter uses toroidal transformers and discrete conductors as shown in Figure A. In addition to the added complexity in BOM (bill of materials) these represent, providing the current sensing function involves assembly of a number of discrete elements, adding both cost and physical bulk. Therefore designers are looking for alternatives within a more highly integrated system. Although printed wiring offers an alternative in the same way as circuit boards replaced discrete wiring in the 1950s, the problem is that the mains load current must transit the assembly requiring a much larger conductor cross-section than is standard with printed circuit processes. "Thick copper" technologies are available, but these are generally accompanied by severe design limitations due to etching undercut and the difficulties of encapsulating the copper. Therefore, in the event logic functions are necessary, the logic circuitry has to be wired using thinner (1/2 oz or 1 oz) copper on a daughtercard. In addition to this disadvantage, according to models based on the IPC 2152 charts a board built

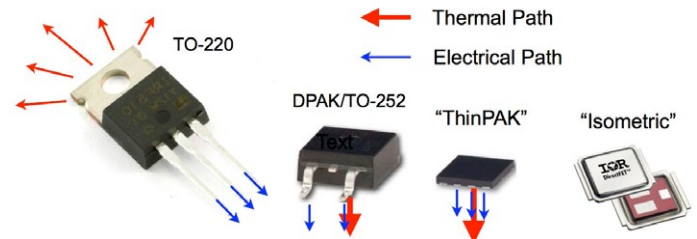


Figure B. Power semiconductor packaging evolution

with 420 µm thick copper would have to be designed with conductors almost 14 mm wide on the innerlayers to manage 90A within a 40°C temperature rise: and all conductors on that layer would be 420 µm thick unless additional processing was used to reduce copper thickness. In comparison, HSMtec solves the same problem using a single 0.5 mm x 12 mm copper strip while all non-power circuitry uses standard 1/2 - 2 oz copper.

Current flow through a conductor causes resistive power losses (I^2R) in the form of heat, and at high current levels the temperature increase becomes a factor in determining ampacity [ampere capacity] because the resistivity of the conductor changes with temperature. The relationship is linear, i.e. resistivity increases proportional to the change in temperature at a rate determined by the temperature coefficient of the conductor:

$$(1) \quad R_T = R_{T_0} \times [(1 + \alpha (T - T_0))]$$

where:

- T = temperature at which resistivity is measured
- T₀ = reference temperature (ambient)
- α = linear temperature coefficient (copper = 0.004)
- R_T = resistivity at measurement temperature
- R_{T₀} = resistivity at reference temperature

For a copper conductor, every 25°C increase in temperature means a drop of about 5% in maximum ampacity due to an increase in conductor resistivity, R_T. Since this presents the probability of further power dissipation and temperature rise, good design practice must consider effective methods not only to control and reduce conductor resistivity, but also to provide low thermal resistance pathways for heat dissipation.

In a printed circuit board ampacity depends on a number of different factors:

- Conductive + convective capability provided by spreading layers, ground layers, stackup
- Ratio of track width to thickness
- Ambient temperature
- Adjacent high current tracks
- Presence and frequency of partial cross-section shrinkage
- Presence, number, and conductive cross-section of plated through holes in series with the conductor

Therefore optimum current design needs to consider more variables than are normally addressed by the IPC 2152 current vs. temperature charts.

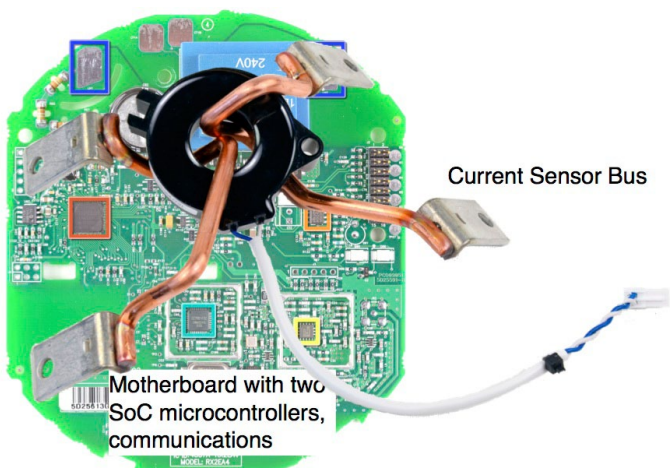


Figure A. RTU Teardown (functional components to scale)
source: iFixit, BPA

The other primary challenge for the RTU is load switching. New generations of power semi-conductors are emerging in response to the need for intelligent power management across an expanding range of applications, from Automotive through Renewable Energy Harvesting, Appliances, Solid State Lighting, and RF Power. All of these applications share the same objective- the efficient and economical management of power. Heavy, bulky electromechanical relays are being replaced by IGBT or MOSFET switches, and these same devices are also used for power control through pulse width modulation of IGBT or MOSFET power stages.

The problems faced by peripheral crosspoints in Smart Grid systems are identical to those involving Digital Power – the need to carry and control loads up through 24 kVA. Power semi-conductors packaged as surface mount devices are enabling significant form factor improvements for power management and control systems, leading to a proliferation of package types such as those shown in Figure. B. In addition to the direct-drive capabilities provided by increasing voltage and current ratings, most of these bring lower assembly costs and improved assembly efficiencies through surface mounting. But, since they're power devices some fraction of that is transformed into thermal energy notwithstanding the improvements in junction efficiencies, and this has to go somewhere or the device will overheat. This is bad news for lifetime and reliability, because semiconductor lifetimes and failure rates are directly connected to temperature of the semiconductor junction. Most predictive models base the relationship between temperature and failure rate on the Arrhenius equation, where temperature can be used as a proportional multiplier. A first-order solution of this relationship suggests that MTTF (mean time to failure) is reduced by half for every 10°C rise in junction temperature.

The combination of surface mount packaging and compact assembly volume means that in most cases the heat can no longer go out to ambient through a heatsink. Surface mounted devices are intended to be small, and they lay flat on the board. So, at least for the first part of the journey, the only way out is down... into the board. Which means that the designer must now consider the need for low-resistance thermal pathways in

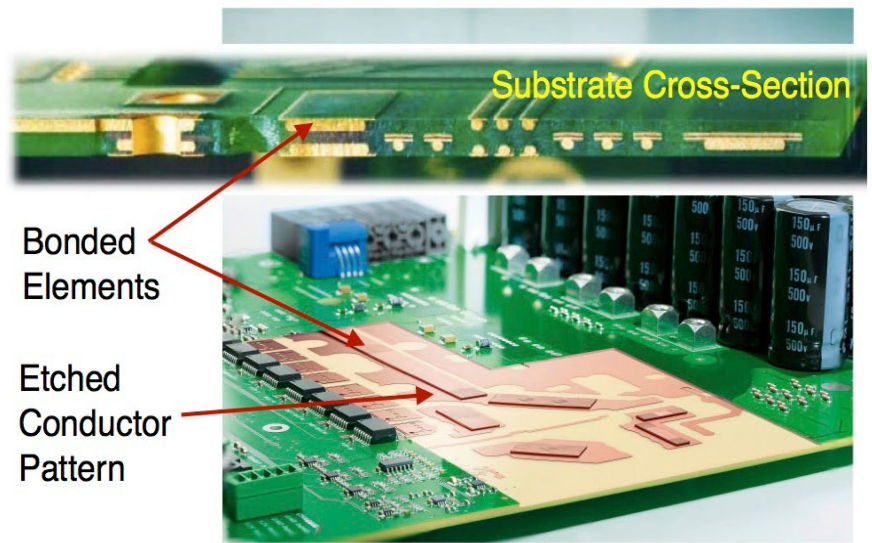


Figure C. HSMtec Concept

addition to the well-known mounting and interconnection functions.

The Solution

The solutions which are emerging offer the potential for replacement of hardware and components formerly used to manage heat and power, and range from simply providing a metal base in the board for heat dissipation to sophisticated solutions combining thermal and power management with high density interconnect and formability. The term “Metal in the Board”, or “MiB” is coming into general use, because these solutions are not metal “core” or metal “base”. They are metal “in” the board.

The manufacturing technologies and capabilities of MiB range from simple three-layer buildups commonly known as “AI-based” or “insulated metal substrate” to complex assemblies using a variety of techniques to provide low thermal and electrical resistance pathways in the board. In every case, the MiB component is providing additional functionality – thermal and/or power management.

In the full version of this article, the author continues to explore practical examples of integrated measurement and switching designs using this technology.



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Analog Tips

DYNAMIC POWER CONTROL MINIMISES POWER LOSS, MAXIMISES TEMPERATURE RANGE

BY DAVID RICE, ANALOG DEVICES

DACs in industrial systems may be expected to drive a wide range of loads. DACs powered by a fixed supply can dissipate significant power on chip, particularly if the load is small or a short circuit to ground. The power dissipated can increase temperatures beyond the recommended operating limits and can be a major concern for systems with large channel density or with higher ambient temperatures.

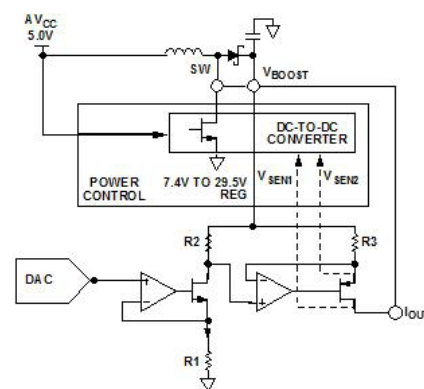
For example, a DAC needs to supply up to 20 mA to a user-defined load in the 100Ω to 1 kΩ range. In this case the minimum supply voltage must be 20V. The maximum power supplied by the DAC is $V \times I = 20V \times 20 \text{ mA} = 0.4W$. If a 1-kΩ load is used, all of the power is consumed by the load, resulting in no lost power. A 100-Ω load consumes only 0.04W, so 0.36W is wasted or dissipated on chip. In some cases, a 0-Ω load is a valid condition, resulting in all power being dissipated on chip.

In a 64-pin LFCSP package, the maximum ambient temperature cannot exceed 125°C. With four channels each dissipating 0.4W, the total power dissipated is 1.6W. The thermal impedance of a 64-LFCSP package is 28°C/W. In the previous example, the temperature rise is $PD \times \theta_{JA} = 1.6W \times 28^\circ\text{C/W} = 44.8^\circ\text{C}$. Therefore the maximum safe ambient temperature is only 80.2°C. Heat sinks can be added to overcome this problem, but this may not be viable due to the required space and cost.

Dynamic power control (DPC) directly addresses this issue. A dc-to-dc converter boosts a 5-V supply to create a 7.5-V to 29.5-V supply. This boosted supply powers the DAC current output driver, which delivers the required power to the load. With a 0-Ω load, the output of the DC/DC converter is 7.5V, its lowest value. The maximum power dissipated in the DAC is only $7.5V \times 20 \text{ mA} = 0.15W$, saving 0.25W compared to the original solution.

With DPC, the maximum power dissipated by four channels (each short-circuited to ground) is 0.6W. The temperature rise

is $PD \times \theta_{JA} = 0.6W \times 28^\circ\text{C/W} = 16.8^\circ\text{C}$. Therefore the maximum safe operating temperature increases to 108.2°C. DPC provides the most benefit in systems having a wide undefined load range, high channel density, and high temperatures that leave little room for large power losses.



The AD5755 four-channel 16-bit digital-to-analogue converter provides voltage and current outputs for programmable logic controllers (PLC), distributed control systems (DCS), and other industrial process-control applications. Dynamic power control regulates the voltage on the output driver, minimising power dissipation with low-value load resistors—and easing thermal management. Each channel can be configured to provide:

- Voltage output, with 0V to 5V, 0V to 10V, ±5V, or ±10V full-scale range and ±0.04% total unadjusted error (TUE);
- Current output, with 0 mA to 20 mA, 4 mA to 20 mA, or 0 mA to 24 mA full-scale range and ±0.05% TUE.

Offset and gain can be individually programmed for each channel. The devices can be used with the on-chip 5 V, ±5-ppm/°C reference or an external reference. Available in a 9 × 9 × 0.85-mm 64-lead LFCSP package, it is specified from -40°C to +105°C and priced at \$13.65 (1000).

Figure 1 shows its current output circuitry, DC/DC converter, and power controller. When the current output is enabled, V_{DS} of the output FET is sensed. This voltage controls the MOSFET in the power control block to regulate V_{BOOST} , which in turn controls V_{DS} as determined by the output current requirement. With the MOSFET switched on, the inductor charges to a value determined by the difference in the actual value of V_{DS} and the required value. When switched off, the inductor discharges into the capacitor and V_{BOOST} pin. This process repeats on each clock cycle. There is one dc-to-dc converter per channel.

David Rice is an Applications Engineer at Analog Devices, Limerick, Ireland. He holds a Masters in Engineering in Embedded Systems from Cork Institute of Technology, Ireland.

GETTING SECURITY RIGHT IN WIRELESS SENSOR NETWORKS

The Internet of Things (IoT) is growing rapidly, and wireless sensor networks (WSNs) are critical to extending the reach of the Internet infrastructure to “everything.” In fact, WSNs are already in use in critical monitoring and control applications around the world. Any loss of security in these systems may have real and direct consequences on efficiency and safety.

Fortunately, the literature on securing wireless systems is readily available, and best practices are well known. Despite this knowledge, the news is filled with reports documenting successful attacks on wireless in general and WSN in particular. Surprisingly, many products on the market do not embrace even the most basic aspects of system security, and many other products with well-intended security fall short of the mark. We document here some of the common mistakes, and their well-known solutions. Wireless security is not trivial, but with rigorous attention to detail, it is possible to build systems that are not vulnerable to wireless attack.

Basics

Security issues are not limited to wireless systems. Indeed, Internet attacks big and small are so common today that they are barely newsworthy. There is a perception that wireless systems are more vulnerable to attack, because anyone with the appropriate radio can communicate with a wireless device from some distance. Of course, on the Internet, anyone with a computer can launch an attack from distances far longer than any radio signal will propagate. The bottom line is that all cyber-physical systems, whether wired or wireless, need to take careful precautions against attack.

Goals

The primary goals of security in WSNs are based on providing three elements:

Confidentiality - Data being transported in the network cannot be read by anyone but the intended recipient.

Integrity - Any message received is known to be exactly the message that was sent, without additions, deletions, or modifications of the content.

Authenticity - A message that claims to be from a given source is, in fact, from that source. If time is used as part of the authentication scheme, authenticity also protects a message from being recorded and replayed at a later time.

Confidentiality is required for not only security-related applications but also for common everyday applications. For example, sensor information regarding production levels or equipment status may have some competitive sensitivity. Sensor data should be encrypted so that only the intended recipient can use it.

Both sensing and command information must arrive intact. If a sensor indicates “the tank level is 72 cm” or the controller

states, “turn the valve to 90 degrees,” it could be disastrous to lose one of the digits in either one of those numbers.

Having confidence in the source of a message is critical. Either of the two messages above could have very bad consequences if they were sent by a malicious attacker. An extreme example is a message such as, “here’s a new program for you to run.”

Consequences

The consequences of poor security are not always easy to anticipate. For example a wireless temperature sensor or thermostat might seem like a product with little need for security. But consider the consequences to product sales due to a newspaper headline describing how criminals used a radio to detect the “vacation” setting on the thermostat, and robbed those houses while the owners were gone. The safest course is to encrypt all data.

In the early days of ZigBee, most networks were run with no security. As a result, in a multi-vendor interoperability demonstration in front of many potential customers, a number of ZigBee networks failed dramatically because they interpreted a command from a different network to be a coordinator realignment message, which told them to change channels. There was no way for the ZigBee networks to determine that the messages were coming from a device that was not in their network. This disastrous behaviour was not the result of an actual attack, but rather a lack of authentication, which led to interpretation of packets from a completely different network.

In industrial process automation, the consequences of an attack may be much more dire than the loss of a customer. If faulty process control information is delivered to the control system,

an attacker could cause physical damage. For example, a sensor feeding data to a motor or valve controller indicating that the motor speed or tank level is too low could result in a catastrophic failure, similar to what was contrived to happen to the centrifuges in the Stuxnet attack.

On a purely practical level, even a failed attack or an academic revelation of a potential weakness is likely to lead to a loss of sales, urgent engineering effort, and a major public relations challenge.

This article continues with a discussion of the tools available to secure data links, beginning with the block cipher (Figure 1) which lets the source encrypt a message so that only the destination (with the same key) can decrypt it.

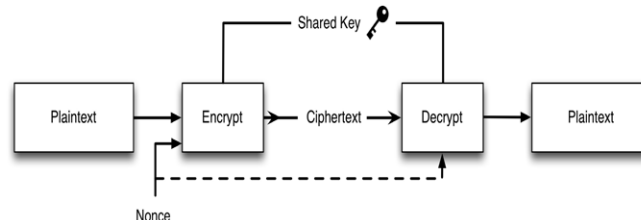


Figure 1 - *Figure 1 A source node uses a block cipher and a nonce and a secret key to encrypt a plain text message, turning it into ciphertext. Only someone in possession of the key can decrypt the message. The nonce may be sent in the clear, or may be implicit from the structure of the protocol, such as a timestamp.*



BIDIRECTIONAL DC/DC CONVERSION ENABLES EFFICIENT BACK-UP POWER CONFIGURATIONS

There are numerous applications in power electronics, where it is advantageous to have power flow in either forward or in reverse directions without the intervention of complex supervisory systems, and without reconfiguring interconnection of major circuit blocks.

The most obvious is to connect batteries as a constantly-connected back-up power source, permitting the battery to be charged from a power bus when offline power is available, and to feed power from the battery to the same bus when it is not. Conventionally, in the traditional uninterruptible power supply, stored energy is used to generate an AC waveform to replace the failed line supply. There are attractions to configuring an equivalent function within the DC distribution level of a power network.

As with all power conversion systems, the architecture of such designs is defined by the location of major functions such as voltage level changing, isolation and regulation. In most of the portable devices we carry, the power bus is effectively the battery potential and is allowed to occupy a range of voltage levels, between that necessary to fully charge the battery, and the minimum the battery can deliver without internal damage. The charging supply and the functional part of the product have a common connection – with refinements – to the battery. Regulation becomes, in effect, part of the application’s function, enabling it to run from any voltage in the permitted range.

For higher power systems, such as larger-scale battery back-up installations or uninterruptible power supplies implemented in DC, this configuration is not satisfactory. There, the requirement is for a constant voltage power bus that is stable at the same level when fed from an offline power supply – powering both client systems and charging the battery – and when the battery comes on-line. Between power bus and battery, therefore, there must be both level-changing and regulation, and, preferably, isolation.

Regulation – maintaining a constant bus voltage over the range of a fully-charged to exhausted battery: or holding the correct level to accurately charge a battery – can be handled by a buck-boost DC/DC converter, and with today’s best zero-voltage-switching architectures, such devices can perform that function with high efficiency. Higher-power battery backup installations will typically operate with a much higher voltage at the systems bus than at the battery, so a large step-up/step down function is indicated. This provides a role for a recently-introduced (by Vicor) functional block termed the BCM or bus converter module.

The BCM was launched largely in the context of power-distribution architectures for, typically, telecommunications or IT server facilities. It provides an isolated DC/DC conversion function that provides a fixed input-to-output voltage ratio. Making a comparison to the role of the transformer in handling AC is irresistible; in almost every respect, the device can be regarded as a “DC transformer”. The BCM, among its other attributes, is bi-directional: power can flow from input to output or vice-versa, with (almost) equal efficiencies – depending on the circuit

configuration, the terms ‘input’ and ‘output’ begin to change their definitions.

In a telecommunications or server rack, power flow through such a module is likely to be resolutely uni-directional; the reversible capability is relegated to interesting footnote. (A typical role might be to step down from a 380V DC bus to the classic telecoms 48V distribution bus level.) However, in a battery backed power system, that feature comes into its own.

The BCM employs the circuit configuration that Vicor calls Sine Amplitude Conversion. A simplified circuit is shown in Figure 1 – this depicts the power paths through the circuit: there will also be control and gate-drive, and other supervisory, functions that are not shown.

The topology is transformer-based series-resonant, and operation depends on maintaining oscillation at the resonant frequency of the tank on the primary side of the power transformer windings, which is labelled T1 in the figure. The control architecture locks the operating frequency to the tank resonant frequency and the four MOSFETs in the H-bridge are synchronously switched so as to sustain a sinusoidal oscillation. The FETs are switched at the zero-crossing points of the sinusoidal waveform, virtually eliminating switching transients, the losses that inevitably accompany a “hard” switching cycle and reducing the generation of high order

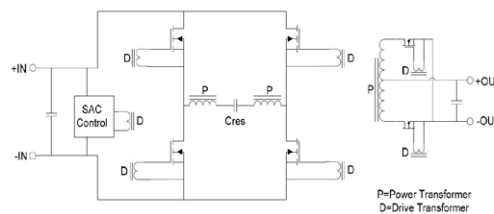
noise harmonics. The current in the primary resonant tank has a sinusoidal shape, and this also contributes in reducing spectral content and provides a cleaner noise signature. The output load, when translated to the primary side, appears in series to the LC tank (series resonant). An increase in output load therefore causes an increase in amplitude of the sinusoidal current

in the tank, hence the name Sine Amplitude Converter. The increase in current amplitude increases the amount of energy coupled into the secondary, countering the load demand. When the load is reduced, the amplitude of the sinusoid decreases, approaching zero under ‘no load’ conditions.

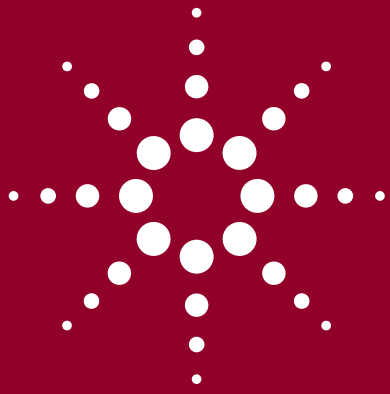
As the amount of energy is only associated with the current amplitude within a small switching period, large reactive, reactive storage elements are not required for this type of topology. The transformer characteristics can be optimised, allowing for a size reduction of the transformer itself, and for high frequency operation, which is also made possible due to the reduced switching power losses. This translates overall into both high power density and efficiency.

The secondary circuit, which could be based on a centre-tapped configuration, as in Figure 1, or a full-bridge of four FETs and a single transformer winding mirroring the primary side, operates as a synchronous rectifier, converting the sinusoidal current to a rectified AC waveform at twice the switching frequency; the output capacitance carries the vast majority of this high frequency current, which is used to maintain an output voltage strictly proportional to the input voltage.

All of which leads to the question; how does the circuit operate when power flows



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Accelerate CAN-Bus Debugging

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Accelerate CAN-bus debugging with CAN-dbc symbolic triggering and decoding

Debugging the Controller Area Network (CAN) buses used in today's automotive systems usually requires investigating both the logical and physical layers. Dedicated CAN bus analyzers exist for debugging at the logical level, but the oscilloscope is the primary measurement tool for testing and debugging the physical layer. The electrical environment in automobiles is naturally harsh with lots of noise and often unexpected transients. The core competence of an oscilloscope is its ability to capture and display details of the noise and infrequent transients that could be producing CAN bus errors.

Using a scope to capture data on the CAN bus

To assist in synchronizing on and identifying specific CAN frames (packets of data), most of today's mid-range and higher-performance oscilloscopes have the ability to trigger on and decode the CAN bus in a hexadecimal and/or binary format (**Figure 1**).

In this example, the oscilloscope has been set up to trigger on frame ID 0x201 (HEX). In addition to decoding the frame ID, the oscilloscope also decoded the 8-byte data field as "0B A8 00 00 27 10 00 00." The measurement capture is successful, but it leaves the engineer with the task of abstracting the result to a result that is meaningful within the context of the application.

Elevating the conversation to human-speak with CAN-dbc

The new CAN-dbc symbolic trigger and decode capability in Agilent InfiniiVision 4000 X-Series scopes offer the best of both approaches: the high-level symbolic perspective of a dedicated CAN bus debugger and the physical layer investigation capabilities of a high-performance oscilloscope.

Figure 2 shows the same measurement but now triggering on and decoding the CAN bus symbolically using the enhanced CAN-dbc symbolic trigger and decode capability. Instead of attempting to manually interpret cryptic hexadecimal codes, the oscilloscope symbolically decodes it in "human language."

In this example, the oscilloscope is decoding a message named "Brake_Torque." In addition, the oscilloscope translates raw bits into signed variables with units as well as encoded states. For instance, Total_Torque = 131.064 kft-lbs, as opposed to 0B A8.

In order for the oscilloscope to decode the CAN bus symbolically, you'll need to import that particular vehicle's .dbc file ("data base CAN") into the scope. All automotive makers have created .dbc files for their vehicles' CAN buses. However, these files are proprietary and top secret, so if you don't have access to one, you'll need to create it. The most common tool used today is Vector Informatik GmbH's CANdb++ software.

Once the .dbc has been imported into the oscilloscope, you have the option of triggering on and decoding the bus in low-level hexadecimal format, high-level symbolic format, or both. This makes testing and debugging the CAN bus quicker and more intuitive.

To learn more about Agilent's InfiniiVision 4000 X-Series oscilloscopes and mixed signal oscilloscopes for automotive applications, visit www.agilent.com/find/scopes-auto.

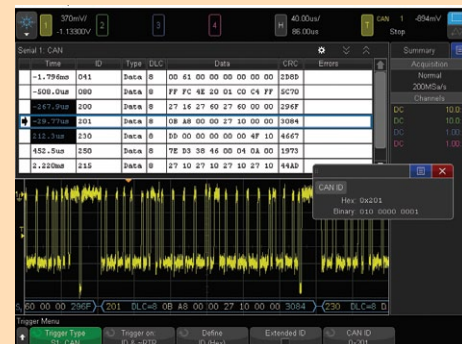


Figure 1:

Triggering on and decoding frame 0x201; the measurement is successful but requires the extra work of abstracting the hex code into application-specific meaning.

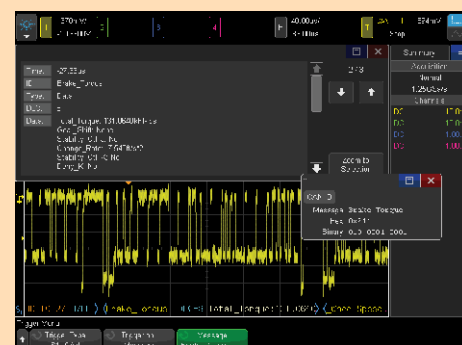


Figure 2:

With symbolic triggering and decoding capability, you can work with human-readable terminology, making troubleshooting faster and much more intuitive.

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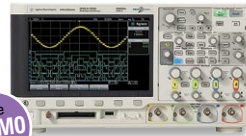
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Model	Description	Features							Max reading rate at 4½ digits (rdgs/s)	Built-in PC Interfaces
		Digits of resolution	DCV, DCI True RMS ACV/ACI	2- and 4-wire Ω	freq/period	diode/cont	cap.	temp.		
U3401A	Dual display. Elegantly simple and affordable DMMs with basic capabilities	4½	•	•	•	•			3	None
U3402A		5½							22	
U3606A	DMM with built-in 30 W power supply. Halves bench/rack space needed for two instruments	5½	•	•					37	USB, GPIB
34450A	Faster measurement speed, ultra-bright OLED with dual display, and basic statistical tools	5½	•	•	•	•		•	190	USB, Serial interface (RS-232), optional GPIB
34460A	Display DMM results in ways you never have before and measure with unquestioned Truevolt confidence	6½	•	•	•	•		•	300	USB, optional GPIB and LAN
34461A									1,000	USB, LAN optional GPIB
34401A	Industry standard for accuracy, speed, measurement ease and versatility	6½	•	•	•	•			1,000	GPIB
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Counts	6,000	10,000	50,000	30,000	4,000
AC bandwidth	1 kHz	2 kHz	30 to 100 kHz	100 kHz	2 kHz
Voltage AC/DC	600 mV to 600 V	1 to 1,000 V	50 mV to 1,000 V	30 mV to 1,000 V*	4 to 1,000 V
Current AC/DC	60 µA to 10 A	1 µA to 10 A	500 µA to 10 A	300 µA to 10 A	40 to 1,000 A
Battery life	500 hours	300 hours	72 hours*	300 hours	60 hours
Additional features	Built-in flashlight, continuity alert with flashing backlight, Z _{Low} non-contact voltage detector with V _{sense} *	Switch counter, harmonic ratio, dual and differential temperature measurements*	20 MHz frequency counter, programmable square wave generator*	Low pass filter, AC and/or DC voltage check, low impedance mode offset compensation* Operational down to -40 °C*	Large 2" jaw size, back light with dual display, ACI, ACV/DCV, diode test, R, C, frequency 400 Ω to 40 MΩ resistance 4 to 4,000 µF capacitance*
Connectivity	IR-USB and Bluetooth				

*Specification available on select models only.

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- USB, GPIB and LAN (LXI) connectivity
- BenchVue software compatible

See **PROMO** Page 2

Model	Key specifications
33509B (Arb optional), 33511B	20 MHz, 1-Ch, 20 MHz pulse
33510B (Arb optional), 33512B	20 MHz, 2-Ch, 20 MHz pulse
33519B (Arb optional), 33521B	30 MHz, 1-Ch, 30 MHz pulse
33520B (Arb optional), 33522B	30 MHz, 2-Ch, 30 MHz pulse
33502A	Isolated amplifier, dual channel, 50 V peak-to-peak

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33600A Series waveform generators



See **PROMO** Page 2

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Model	Key specifications
33611A	80 MHz, 1-Ch 660 MSa/s arb, 60 MHz pulse
33612A	80 MHz, 2-Ch 660 MSa/s arb, 60 MHz pulse
33621A	120 MHz, 1-Ch 1 GSa/s arb, 100 MHz pulse
33622A	120 MHz, 2-Ch 1 GSa/s arb, 100 MHz pulse

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53210A	350 MHz RF frequency counter, 10 digits/s
53220A	350 MHz universal frequency counter/timer, 12 digits/s, 100 ps
53230A	350 MHz universal frequency counter/timer, 12 digits/s, 20 ps

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- Frequency range: 9 kHz to 3 GHz
- DANL: -148 dBm with pre-amp on
- RBW: 10 Hz to 1 MHz
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- DANL: -152 dBm typical, with preamp on
- RBW: 10 Hz to 3 MHz
- 7 GHz tracking generator, built-in VSWR bridge
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- Free remote control PC software
- BenchVue software compatible



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- Stimulus and response tester
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34970A/72A plug-in modules


Model	Key specifications
34901A/02A/08A multiplexers	Up to 300 V, 16, 20, or 40 channels
34903A GP switch	300 V, 20 actuator channels
34904A matrix	4x8 matrix
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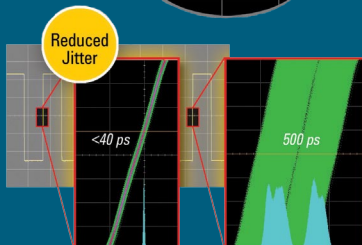
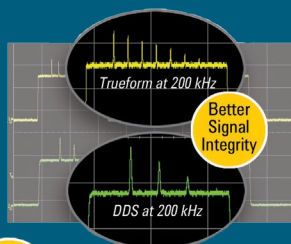
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DESIGNING FOR IOT—PART III—INTERNET USAGE AND PROTOCOLS

The previous two articles in this series ([here](#), and [here](#)) described the hardware and software required to build an IoT device. These devices (the “Things” in the Internet of Things) are an essential part of an IoT system. There are two more building blocks to complete our system design. In this segment, I will look at the Internet, its usage by IoT devices, and the existing and new Internet protocols supporting the explosive growth of this new industry.

The Internet

The Internet is the sum of all the network equipment used to route IP packets from a source to a destination. The World Wide Web, by comparison, is an application system that runs on the Internet. The Web is a tool built for people to exchange information, and in the last twenty years, we have developed and refined the Web so that ordinary, non-technical people can use the Internet easily and productively. The human interface for the Internet now includes e-mail, search engines, browsers, mobile apps, Facebook and Twitter, and other popular social media.

By comparison, in IoT, the idea is for electronic devices to exchange information over the Internet. But these devices don't yet have the machine equivalent of browsers and social media to facilitate communication. IoT is also different from the Web because of the speeds, scales, and capabilities that IoT devices require in order to work together. These requirements are far beyond what people need or use. We are at the beginning of the development of these new tools and services, and this is one of the reasons why a definition for IoT is difficult to lock down. Many visions about what it can, or could be, collide.

TCP/IP Protocol Stack

The TCP/IP protocol stack is at the heart of the Internet and the Web. It can be represented using the OSI seven-layer reference model, as illustrated in Figure 1. The top three layers are grouped together, which simplifies the model.

The following is a quick description of the important layers from the perspective of embedded system integration:

Physical and Data Link Layers

The most common physical layer protocols used by embedded systems are:

- Ethernet (10, 100, 1G)
- WiFi (802.11b, g, n)
- Serial with PPP (point-to-point protocol)
- GSM 3G, LTE, 4G

Network Layer

This is where the Internet lives. The Internet — short for Inter-Net-work — is so named because it provides connections between networks, between the physical layers. This is where we find the ubiquitous IP address.

Transport Layer

Above IP, we have TCP and UDP, the two transport protocols. Because TCP is used for most of our human interactions with the Web (e-mail, Web browsing, etc.), it is often believed that TCP should be the only protocol used at the transport layer. TCP provides the notion of a logical connection, acknowledgement of packets transmitted, retransmission of packets lost, flow control, all of which are great things. But for an embedded system, TCP can be overkill. This is why UDP, even if it has long been relegated to network services such as DNS and DHCP, is now finding its place in the domains of sensor acquisition and remote control. If you need some type of management of your data, you can even write your own lightweight protocol on top of UDP and avoid the overhead imposed by TCP.

UDP is also better suited than TCP for real-time data applications such as voice and video. The reason is that TCP's packet acknowledgment and retransmission features are useless overhead for those applications. If a piece of data (such as a bit of spoken audio) does not arrive at its destination in time, there is no point in retransmitting the packet, as it would arrive out of sequence and would garble the message.

TCP is sometimes preferred to UDP because it provides a persistent connection. So to do the same thing with UDP, you have to implement this feature yourself in a protocol layer above UDP.

When you are deciding how to move data from the Thing's local network onto an IP network, you have several choices. Because the technologies used are familiar and available from a wide range of sources, you can link the two networks via a gateway, or you can build this functionality into the Thing itself. Many MCUs now have an Ethernet controller on chip, which makes this an easier task.

This article continues with a summary of protocols for the IoT — click the link.

OSI Seven-Layer Model

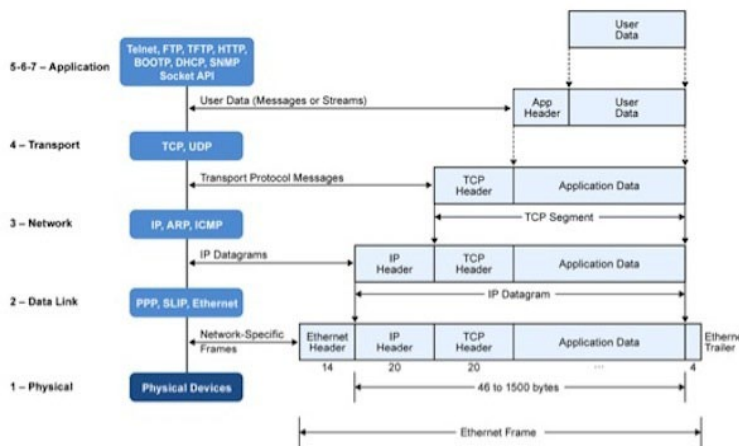
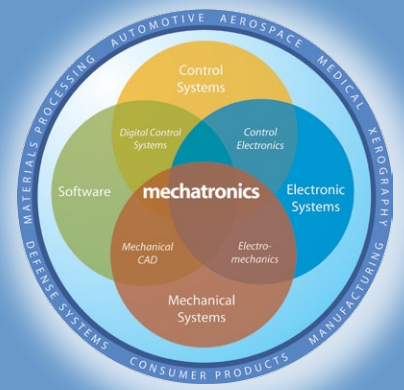


Figure 1- The TCP/IP reference model



MECHATRONICS IN DESIGN

FRESH IDEAS ON INTEGRATING MECHANICAL SYSTEMS, ELECTRONICS, CONTROL SYSTEMS, AND SOFTWARE IN DESIGN



Full step, half step, or micro-step?

By Kevin Craig

A step motor is an open-loop, brushless, digital actuator driven in fixed angular steps. The hybrid step motor (Figure 1) is most common and has magnetically-permeable teeth on both the stator and rotor. The sources of magnetic flux are the stator windings and the rotor permanent magnet (which gives it a detent torque when not energised); high magnetic flux leads to high tangential forces between rotor and stator teeth, resulting in high torque. There are two stator windings, each situated on alternating poles; successive poles of each winding are wound in the opposite sense.

Hybrid motors have four phases: a bipolar (unifilar) motor uses current reversal in each winding, while a unipolar (bifilar) motor uses twice the number of windings. The step angle is 90 degrees divided by the number of rotor teeth, with 1.8 degrees most common; four phase excitations (four steps) correspond to one rotor-tooth pitch. For a well-designed step motor, the stator/rotor iron should reach magnetic saturation at the rated winding current. A step-motor system is a mechatronic system and its performance is determined by the motor, the motor driver, the load connected to the motor, and the desired motion trajectory.

In a hybrid step motor, torque is linearly proportional (constant k_T) to the phase current. The data-sheet holding torque T_H is usually obtained with two phases energised at the rated current I_r . The motor torque constant k_T for one coil is obtained by dividing T_H by $(1.414)I_r$, since T_H results from the vector sum of torques from each phase.

Resistance (R) and inductance (L) are the two inherent physical characteristics of a step-motor winding, and these limit the possible performance of the step motor. R is responsible for the major share of the power loss and temperature rise of the motor. L makes the motor winding oppose current changes

and therefore limits high-speed operation.

To drive current through a winding, use as high a voltage as possible and keep the inductance low. The driver circuit has two major tasks: (a)



change the current and flux direction in the phase windings, and (b) drive a controllable amount of current through the windings enabling as short current rise and fall times as possible for good high-speed performance.

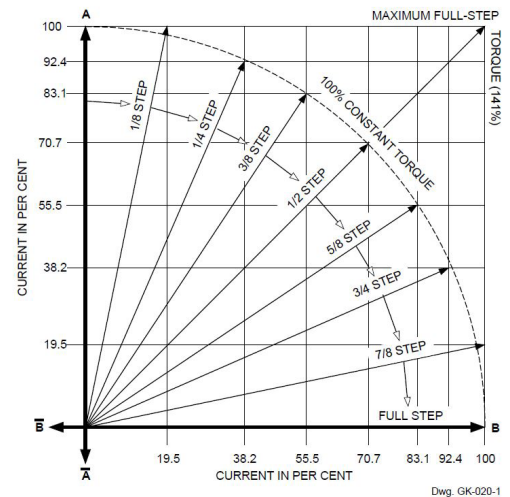


Figure 2 source, Allegro Microsystems.

The chopper driver provides an optimal solution both to current control and fast current build-up and reversal. Use a supply voltage several times higher than the nominal voltage of the motor; the current rise rate will increase substantially. Control the duty cycle of the chopper, using a current-sensing resistor, to achieve constant current regulation. This results in precise control of the developed torque and minimises power dissipation.

Step motors can be driven in several modes: full-step, half-step, or micro-step (quarter and eighth stepping are common). Full-step operation can be achieved by one-phase-on excitation at a time at the rated current. Maximum torque is achieved in the full-step mode with both phases fully energised at the same time for each step.

Figure 2 shows constant-torque vectors for the different step modes, along with the phase currents required. To accurately control the stable, zero-torque position of the motor, specific phase currents must be applied. These desired phase currents follow from three requirements: (a) the torque of the motor equals zero, (b) the slope of the torque vs. position curve has a negative slope (i.e., a stable equilibrium position), and (c) the currents result in a constant power dissipation. All these requirements are met by varying the phase currents as sine and cosine curves.

Step motors are everywhere and are just one component in an integrated system. Fundamental understanding is essential.

ANALOGUE COMPONENTS PLUS ARM MCU CORES TO MEET EMBEDDED CHALLENGES

The design of tomorrow's embedded systems presents complex challenges given the aggressive goals of improvement in areas of performance, cost, power, size, new features, and efficiency. An emerging design option to address these complex problems lies in analogue components intelligently integrated with ARM microcontroller cores.

Smart integration of high performance analogue components (amplifiers, ADCs, DACs, voltage references, temperature sensors, wireless transceivers etc.) and 32 bit processor cores from ARM with the right digital peripherals can address goals that discrete solutions cannot. In order to create the optimum analogue microcontroller solution, a strong knowledge of the overall system along with the availability of the right intellectual property (IP), and expertise in that intellectual property, is required. Chip designers and system engineers specifying the features of these integrated devices must have an exceptional understanding of the end application requirements. This domain knowledge is critical and includes a solid understanding of board level requirements such as form factor, temperature ranges, manufacturing, power consumption, cost, and complementary components in the signal chain.

Availability of the right IP provides a strong starting point for meeting system level goals. This starting point is needed to keep the development period of the analogue microcontroller short. Increasingly, the acquisition/creation and implementation of the IP itself, appropriate for the application, needs to be facilitated by the semiconductor manufacturer. This IP then needs to be modified to meet two requirements, in particular. The first is to maximise system level benefits by optimising performance and operation based on the needs of the primary target application. The next is to optimise the IP to work very well and very easily with the other complementary IP blocks in the analogue microcontroller.

And finally, there needs to be the opportunity at a business level for collaboration, combining the expertise and knowledge of the system manufacturer and semiconductor manufacturer resulting in an optimised, unique design.

Analogue MCU applications

There are many applications that can benefit from a device that integrates high performance analogue with ARM microcontrollers including temperature sensing, pressure sensing, gas detection, solar inverters, motor control, health care vital signs

monitoring, automotive monitoring systems, and gas/water/ electric meters. This article will look at two applications areas where integration of optimised high performance analogue and ARM microcontroller cores leads to significant benefits in cost, power, size, and performance:

- 1) Inverters for solar photovoltaic systems (PV) with goals of increased efficiency, bill of material (BOM) cost reduction, and integration of intelligence to support interfacing to the smart grid.
- 2) Motor Control, with the goals of improved efficiency for environmental benefits and cost reduction.

Note that while these smartly integrated mixed signal devices are optimised for particular end-applications, they can also work well for numerous adjacent applications having similar functional requirements to the primary target application.

Solar photovoltaic inverters: : context - cost reduction, and the smart grid

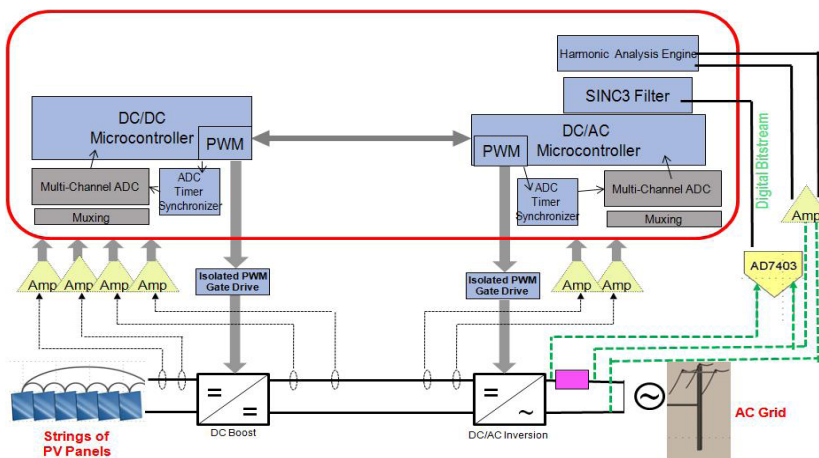


Figure 1. Block diagram of two stage solar PV inverter system; area in red shows blocks targeted for smart integration.

To better compete against traditional energy sources such as natural gas, coal, and oil, cost reductions of solar PV generated electricity is best achieved by both increases in efficiency and reduction in system BOM costs. As cost/efficiency of the panels themselves is trending down, new technologies also promise advances for solar PV inverters - the interface between the power generated by a solar panel and the grid. These new technologies include

NPC topologies 3 level/ 5 level / multilevel, and high frequency switching topologies using fast power transistors based on silicon carbide (SiC) and gallium nitride (GaN) materials.

Figure 1 shows a two stage solar PV inverter system. Power from the panels, essentially a DC source, is converted to AC for the grid. The first stage is a DC to DC conversion that raises the voltage level so it is compatible with the peak voltage on the grid. The second stage is a DC to AC conversion. The area in red shows the low voltage circuit control components that, when integrated into a single analogue microcontroller chip, give benefits at a system level.

The authors continue the expanded version of this introduction by looking in more detail at the level of performance required of the analogue blocks in this mixed-signal scenario.



SIZE TRENDS IN MEDICAL SENSING; COMPACT TECHNOLOGY MEETS PATIENT NEEDS

Medical device design engineers face unprecedented opportunities and challenges; one of the most pressing challenges is to create sensor elements which keep pace with the miniaturisation occurring in nearly all medical devices, from simple blood pressure monitors to complex heart-lung machines.

Applications range from patient transport, through the operating theatre to home-care;

- Patient transport, intake and ambulatory care environments - the smaller the equipment is, the earlier it can reach the patient and the greater the likelihood it can be deployed directly at first-response sites. Likewise, smaller respirators, infusion pumps and vital sign monitors help hospitals to improve the quality of in-room and ICU care.

- The operating theatre - space in an operating theatre is always at a premium. Compact monitors, pumps, and suction equipment give a scrub team better access to both the patient and the monitors, life support and treatment equipment.

- Patient mobility and home-care - highly portable equipment is critical for patients recovering in hospital and returning home where mobility will give them greater autonomy and comfort and, in many cases, a speedier recovery.

Sensor technology meets compact design requirements

A key focus of R & D in this field is space-saving sensors and the integration of multiple sensor elements in a single package. Advanced integration techniques have allowed sensors to be placed within small surgical devices and other applications, in configurations which were previously considered impossible. A number of technology developments are contributing to meeting medical needs.

Board-mountable sensor packages

Sensor platforms that offer several options for mechanical interfaces, mounting, packaging, and I/O options to give medical equipment designers new degrees of freedom when designing medical equipment are critical. For example, pressure sensors that provide several options for mating connections (port styles), packaging (DIP, SIP, surface mount), and outputs (analogue or digital) which can be used to satisfy their application demanding functional, cost and board space requirements.

The multiple benefits offered by sensors presented as board-mountable packages have made them one of the most popular space-saving components for medical and industrial designs. In the case of sensors which measure fluid pressure or flow, board-mount packaging enables the sensing element to be firmly attached to the device's printed circuit board (PCB) as close as possible to the patient and/or the liquid media being sensed (e.g. blood, chemicals or water).

This is especially important in certain applications, such as dialysis machines, which require precise and accurate mea-

surement of dialysate (one of the fluids involved in the dialysis process) and venous pressure to ensure a patient's safety and comfort during treatment. Accurate measurement of pressures in the fluid and blood flows helps ensure that an over-or-under pressure situation does not occur, conditions which can result in either burst blood vessels or air bubbles in the dialysis feed line. For these types of applications a board-mounted package can help provide the close proximity the pressure sensor needs to produce accurate, precise measurements and better response times to changes in the system.



Figure 1- Modern medical devices, such as these infusion pumps, require compact sensors compliant with the stringent standards which govern medical materials safety.

Besides ensuring accurate and precise measurements, board-mounted sensors enable simpler, more reliable designs which can be quickly assembled using automated equipment. Pressure and flow sensors are typically available in several board-mount package styles, many of which offer options for different orientations for their integrated ports. This can be very helpful for a design that needs a clear path for the tubes which connect the sensor with whatever medium it is monitoring.

Packaging options

Packaging options which combine the sensor port and a pre-integrated manifold can provide additional space savings for some applications by eliminating the tubing and related connections between the sensor/port assembly and its target medium resulting in a simpler, more compact design.

The direct connection afforded by manifold-mounted packaging also eliminates many of the problems in conventional designs where clogs, leaks and other types of failures can occur. Manufacturers often find that by eliminating the trial-and-error required to optimise a port's performance, using pre-engineered manifolds can provide significant savings in a design project's engineering labour costs and development schedule.

Multi-sensor / multi-function packages

Many medical devices can benefit from integrated sensor solutions which combine multiple functions, such as temperature and humidity, or temperature and pressure. Multi-sensor solutions can be implemented by either co-packaging two or more sensor elements or integrating separately-packaged sensors within a compact higher-level assembly.

Optimising the solution to a single package can ensure tighter correlation between devices and can lead to savings in space and installation time. Honeywell supplies a single integrated, warranted solution that may in the past have required multiple suppliers, thereby reducing the need to manage multiple part numbers for a given function.

This article concludes with application examples of sensors that combine two functions – for example, temperature and humidity – in one package – click the link.




designideas

READERS SOLVE DESIGN PROBLEMS

Smart ripple canceller offers near-zero dropout

by Louis Vlemincq

 Ripple cancellers, also known as ripple-eaters, gyrators, or electronic filters, are useful when a supply needs to be clean but the absolute supply voltage is unimportant. A typical application of these circuits is in class-A power amplifiers. Compared to a linear regulator, they waste less power since they adapt themselves to the input voltage. There are however some inevitable losses: at the very minimum they have to drop the peak expected ripple voltage, and they also need some operating margin themselves. All of this easily amounts to several volts, leading to a corresponding power waste.

In theory, a purely passive filter could do better, but even with a large inductor, there will always be Joule's losses. In addition, such a filter would be costly and offer a less than perfect ripple rejection.

This Design Idea combines both methods, and also adds some tricks of its own to achieve a near-perfect, hybrid filter.

The circuit is based on transformer T1, having its secondary in series with the supply to be filtered. The secondary voltage is therefore subtracted from the input voltage, and if it exactly equals the ripple voltage, perfect cancellation will occur, yielding a pure DC output.

The transformer's primary is connected to an error amplifier generating a suitable voltage. Basically, two strategies are possible: open-loop and closed-loop. Both can be made to work, and have their specificities: the open loop method samples the input ripple, scales it accurately, and sends it to the transformer. The effectiveness of the cancellation depends on the accuracy of the passive components.

The closed loop circuit samples the output and adjusts the error voltage so as to cancel any ripple. This technique is less reliant on accuracy, but as with any servo system, the accuracy of the process depends on the loop gain, which in turn can cause stability issues. The circuit presented here is of the closed-loop variety.

One objection to the use of a transformer is the large DC current flowing through its secondary; normal, ungapped transformers don't tolerate much DC without saturation, and gapped transformers are much bulkier. Here, the problem is addressed in an elegant manner: the transformer works in compensated mode, the primary receiving exactly the same DC amp•turns as the secondary. To this end, the error amplifier works in class A, and its bias current is servo-ed to the output current. The current is sensed by R5, and Q1 to Q3 mirror a scaled version through R2 and R3. This ensures that T1 sees zero net flux at all times. Q2 is the error amplifier, and it receives the error voltage on its emitter, via C4.

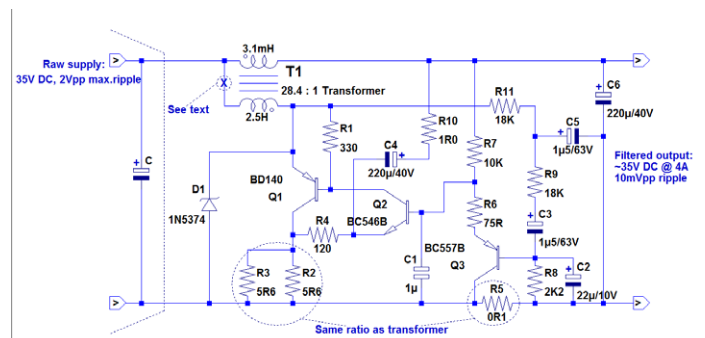


Figure 1. Ripple canceller

Stability issues cannot be taken lightly in such a circuit: combining a lot of gain with many reactive components, the circuit has a number of opportunities to turn into an oscillator at a variety of frequencies. The low-frequency compensation is ensured by R9, R11, C5, and C2. C1 takes care of the high frequency department. It has been found in practice that the circuit remained stable without it, but I recommend leaving it in.

Less obvious stability problems can also occur when the input supply is not "stiff" enough. That can happen at light loads, when the internal resistance becomes higher. When the circuit tries to compensate for a drop in the input voltage, the amplifier draws momentarily more current, and if this causes the input voltage to drop further, it results in a positive reaction and instabilities, causing motor-boating. The phenomenon is akin to a right half-plane zero and is almost impossible to compensate away using conventional methods without ruining at the same time the performance of the circuit.

In moderate cases, a simple filter in series with the primary may be sufficient (Figure 2A). In difficult cases, an active circuit is required (Figure 2B).

This circuit works by duplicating the current drawn by the error amplifier: R2, R5, R6, & R7 are arranged in a bridge, and since R2 is about half the value of R7, Q1 and Q2 try to make R2's current double R7's. But C2 delays the action, which means that short-term, the input

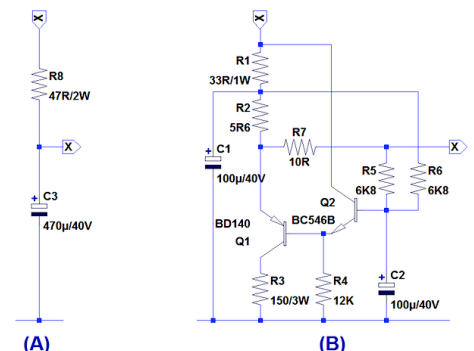


Figure 2. An extra filter may be required in some cases

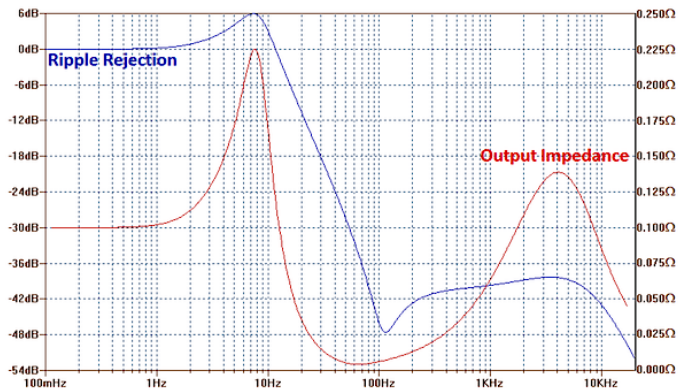


Figure 3. Output impedance and ripple rejection

current is invariable, eliminating therefore the RHP zero. The double-current-law ensures the circuit is never starved dynamically. Note that most of the time, this circuit will not be required.

Implementation notes

The maximum ripple rejection capacity is set by T1's ratio: $n = 200/(\% \text{ ripple } P-P)$.

This in turn sets the ratio of $R_2 \parallel R_3$ to R_5 .

The transformer's magnetising inductance must be large enough to allow the amplifier to develop its full swing. This mandates $L_m > (n \cdot V_{IN}) / (2\pi f \cdot I_{OUT})$.

It is advisable to provide some margin with respect to these values, in particular the magnetising inductance L_m , which should be more than twice the minimum.

Performance

Figure 3 shows the rejection and output impedance curves. Rejection is greater than 40 dB for the pertinent frequency range, with a maximum at 100 Hz exceeding 46 dB. The output impedance too is impressive: the gain of the amplifier helps not only the ripple rejection, but it also actively reduces the output impedance.

The only losses are caused by R_5 and the resistance of the transformer's secondary. They may not be zero, but they are so low that the circuit has a negative drop-out for almost 50% of the time!

This remarkable performance only requires a moderately sized transformer. Let us take an unfavourable example: a 50V/5A supply having up to 10% ripple. The secondary/core must have a high enough $V \cdot s$ product to accommodate about 2 VRMS ripple. With the 5A current, this results in a 10 VA rating. But since the ripple is at twice the mains frequency, this means that 5 VA is in fact sufficient for this heavily rippled 250W supply.

About the author

Louis Vlemincq started electronics as a young teenager, first as a hobby, then as a regular job after graduating. He has touched to almost every field of electronics: audio and video design and maintenance, automotive, industrial control, lasers, telecommunications. He currently works as a physical layer specialist for DSL technologies (copper) at Belgacom, the main telecom operator in Belgium.

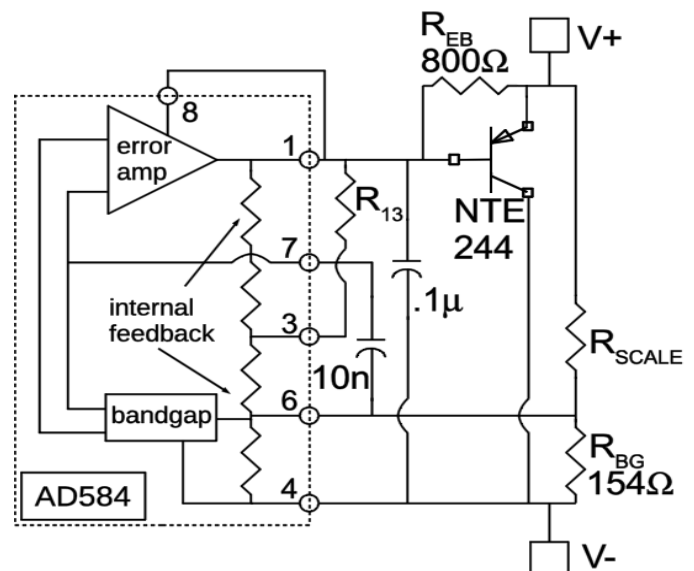
High-power shunt regulator uses BJT and reference IC

by Chris Toliver



Some voltage references can be used as shunt regulators, either by tying V_{IN} and V_{OUT} together or by leaving V_{IN} open. These devices are limited to low currents, however, with a typical limit of around 10 mA. Standard Zener diodes serve the same function, and can operate up to about a watt, but they suffer from high series resistance.

The AD584 voltage reference, along with an external pass transistor, such as the NTE-244, allows the synthesis of shunt regulators that can handle as much as 50W. The circuit shown can be used to clip high-current, long duration, over-voltage pulses – or it can be used as a floating series voltage drop. The AD584 voltage reference combines a precise band-gap reference cell, an error amplifier, and a feedback network. Direct access to the band-gap's input allows the internal feedback network to be overridden via the external pass transistor and feedback network. The result is a stable voltage between the V_+ and V_- terminals. R_{13} and R_{EB} are included to properly bias the AD584. The 10 nF and 0.1 μ F bypass capacitors are included for stability.



R_{SCALE} can be calculated from:

$$V_{OUT} = V_+ - V_- = V_{BG} \times (R_{SCALE} / R_{BG} + 1)$$

where $V_{BG} = 1.22V$.

From the data sheet, the internal feedback resistors in the AD584 are 36 k Ω and 12 k Ω , and the desired voltage on pin 3 is $V_- + 2.5 V$. Thus, R_{13} can be calculated from:

$$12k\Omega / (12k\Omega + (36k\Omega \parallel R_{13})) \times (V_+ - V_{EB}) = 2.5V$$

This equation simplifies as:

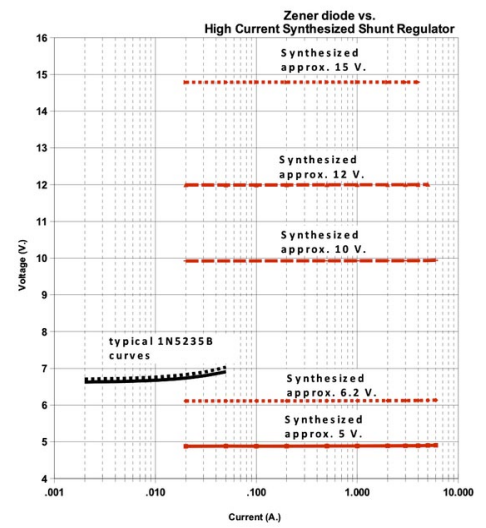
$$R_{13} = -36k\Omega \times (V_+ - 2.5 - V_{EB}) / (V_+ - 10 - V_{EB})$$

For the NTE-244, $V_{EB} = 1.5$ V, so the equation becomes:

$$R_{13} = 36k\Omega \times (V_+ - 4) / (11.5 - V_+)$$


The graph shows the results at five example voltages. The circuit has no problem sinking 5A at lower voltages, or handling 50W to 60W at higher output voltages, subject of course to

proper heat sinking and temperature derating of the NTE-244 power device. Note that the circuit regulates far better than a Zener diode while operating over a much higher current range.



Simple capacitance meter bins surface-mount parts

by Raju Baddi

 This Design Idea describes a simple two-chip CMOS circuit that can sort capacitors into 20 bins over a wide range (100 pF to 1 μF), using 10 LEDs to display the value range. The circuit is power efficient and can be run using two CR2032 cells. As such, it can be built into a handheld probe.

The heart of the circuit is the RS flip-flop using 4093 NAND gates along with transistors Q1 and Q2, which discharge the reference and test capacitors respectively. The reference capacitor (C_{REF}) and the test capacitor (C_x) are charged from zero volts, followed by a reset pulse applied to the bases of Q1 and Q2. Depending on the values of the capacitors and their respective series resistors, either C_x or C_{REF} reaches the gates' V_T before the other; accordingly the outputs of the RS flip-flop are set/reset. The outputs are so wired such that when C_{REF} reaches V_T before C_x , a clock pulse is applied to the CD4017 counter, whose outputs (Q0-Q9) charge C_{REF} through one of 10 different series resistor values (R0-R9).

The master clock that runs the circuit is derived using a single

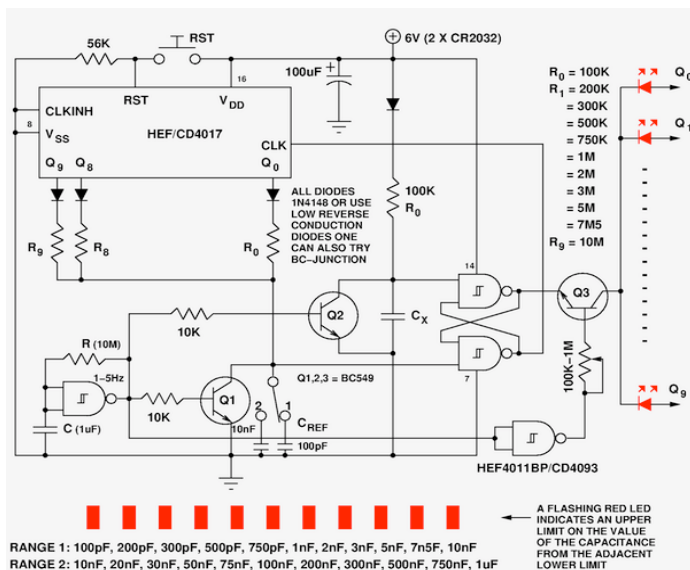


Figure 1. Capacitance meter schematic. A 4011 NAND can exhibit some hysteresis, but a 4093 is recommended.

4093 Schmitt NAND gate. This steps the 4017 decoded decade counter, the flip-flop “comparing” the voltage ramps across C_x and C_{REF} while charging C_{REF} through the different values. When C_x reaches V_T before C_{REF} , then 4017 is not clocked, and the appropriate LED starts flashing indefinitely. Depress the reset switch to take another reading, which resets the 4017 and selects the minimum resistor value, R0. There are two ranges, each divided into 10 sections, which cover 100 pF-10 nF and 10 nF-1 μF. The range is selected by an SPDT switch which connects a C_{REF} of either 100 pF or 10 nF.

A particular flashing LED indicates that the value of the test capacitor lies in the range between it and the next lower LED. Q3 takes care of lighting the LED in the appropriate phase of the master clock. The anodes of the 10 LEDs are connected to the outputs (Q0-Q9) of the CD4017. It seems that lower values of charging resistors can result in more reliable readings due to smaller errors in the charging current (contributed mainly by reverse conduction in all the diodes). R0-R9 can be scaled appropriately, together with an inverse scaling of the master clock frequency.

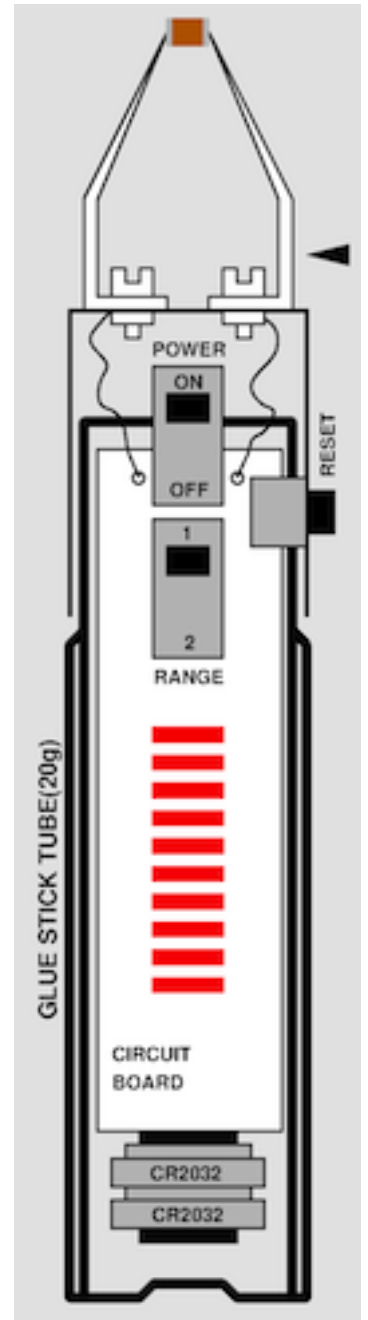


Figure 2. A possible handheld probe construction example using a glue stick tube.

Wireless bicycle brake light

by John Craig



This Idea was one of the runners-up in the Texas Instruments LDC1000 inductive sensor design contest.

My submission video shows the new Texas Instruments LDC1000 attached to the rear wheel fork of a bicycle, where it senses the spokes as the wheel rotates. This proof-of-concept demonstration shows how perfect this sensor is for my goal of an improved bicycle brake light that has many advantages. I'm passionate about getting this invention completed and on the market as soon as possible, where it can help prevent some of the many injuries and deaths to the hundreds of millions of the world's bicyclists each year.

My first LucidBrake invention used a 3-axis accelerometer, plus a complicated microprocessor algorithm to detect bicycle deceleration while eliminating most bumps, rotations, and variable mounting angles. It works, but it's not perfect, and in my quest for something even better I've often asked myself "How can I detect velocity directly, without having to do all these problematic and inexact calculations from the acceleration data?"

With perfect timing, the new LDC1000 inductance to digital converter from Texas Instruments provides the ideal solution!

As shown in the video, with no adjustments to sampling rate, or any of the other register settings, the TI LDC1000 worked perfectly to detect spokes as they transition near the sensor. During the industrial design and engineering that will be required to bring this invention to market we'll optimise the settings, the coil shape, size, and other details, but I was thrilled when it worked "as is" right out of the box!



So why do I consider this to be the perfect answer to my quest for building the perfect bicycle brake light? Consider these facts: No optics to get dirty. No expensive rare earth magnets. Nothing needs to be added to the bicycle's wheel in any way to detect rotations. No wiring to the bicycle's braking system at all. Just attach it to a rear fork... and it just works!

The sampling rates available on the TI LDC1000 provide hundreds to thousands of readings for each spoke's transition near the sensor, even for the fastest bicycles. The threshold output on the INT pin provides the perfect way to determine very accurate bicycle velocity - a simple microcontroller count between pulses does the trick. When velocity is decreasing at a significant rate, the brake light comes on. Couldn't be simpler! This will work independent of hills, slopes, or bumps, providing an instantaneous and absolutely perfect way to light the ultra-bright brake light LEDs when the bicycle is slowing down.

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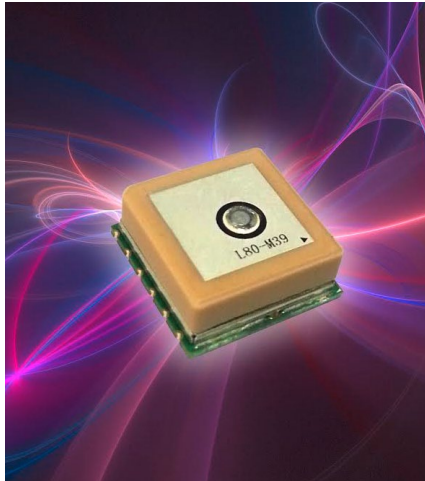


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productroundup

GPS module integrates patch antenna

Distributor MSC Technologies is stocking the L80 module from Quectel, an ultra-compact POT GPS module measuring 16 x 16 x 6.45mm including the integrated patch antenna. Based on the MTK3339 platform from Mediatek it supports 66



acquisition and 22 tracking channels. The module draws 20 mA in tracking mode, and has input sensitivity of -165 dB in tracking mode and -148 dBm in acquisition mode. It is suited for industrial applications due to its working temperature of -40 to +85 °C. EASY Assisted GPS technology enables a first rapid localisation and high positioning accuracy even at indoor

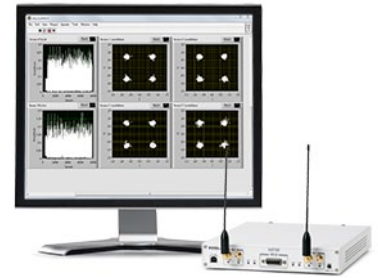
signal level. Satellite data can be automatically calculated with the ephemeris data from the past 3 days, which are stored in internal flash memory. In order to achieve an optimal balance between positioning accuracy and energy consumption, the ON-/OFF-Time can also be adjusted adaptively by Always Locate technology.

Complete article, here



MIMO-capable wireless prototyping platform

An integrated software defined radio solution for rapidly prototyping high-performance, multichannel wireless communication systems, the NI USRP RIO platform is built on the NI LabVIEW RIO architecture and combines a high-performance 2 x 2 multiple input, multiple output (MIMO) RF transceiver capable of transmitting and receiving signals from 50 MHz to 6 GHz with an open LabVIEW programmable FPGA architecture. Wireless engineers can use this technology to rapidly prototype real-time wireless communications systems and test them under real-world conditions. They can also more rapidly prototype increased-capability wireless algorithms and systems, and reduce time to results using what NI terms the only complete platform to take full advantage of a graphical system design approach. The USRP RIO family delivers high-performance, real-time processing capability with the Xilinx Kintex-7 Series FPGA.

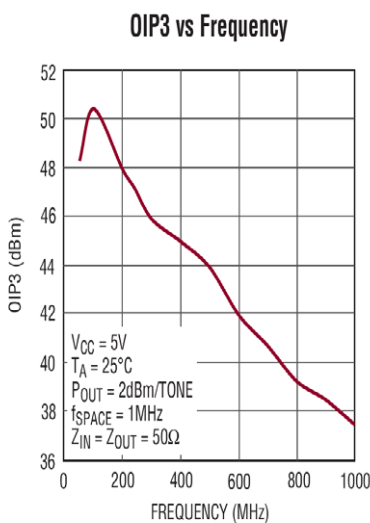


Complete article, here



50-Ω 20dB to 2 GHz gain block

TC6431-20 is a 20 MHz to 2 GHz single-ended input and output fixed gain amplifier offering 46.2 dBm OIP3 (Output Third Order Intercept) and 2.6 dB noise figure. Its OP1dB (Output 1 dB Compression Point) is 22 dBm. Two grades are offered, an A-grade version that is 100% tested and guaranteed



to have a minimum of 42.2 dBm OIP3 at 240 MHz, and the B-grade version offering a typical OIP3 of 45.7 dBm at the same frequency. Both input and output are internally 50Ω matched from 20 MHz to 1.4 GHz, with a frequency response of 20 dB power gain and a flatness of better than 0.5 dB. Internal 50Ω matching simplifies design and enables easy cascading, using minimum external components. Each amplifier needs only

an input and output DC blocking capacitor, plus a choke to bias its open collector output.

Complete article, here



Broadband vector network analyser covers 70 kHz to 145 GHz

Anritsu's VectorStar ME7838D broadband system provides frequency coverage of 70 kHz to 145 GHz in a single sweep using a coaxial test port. The VectorStar ME7838D can conduct a single sweep on a device over multiple RF, microwave, and millimeter wave (mm-wave) waveguide bands, allowing engineers to more accurately characterise devices. The key enabler for broadband operation to 145 GHz is the Anritsu-developed MA25300A Non-Linear Transmission Line (NLTL) module, that extends the frequency range of previous Anritsu NLTL modules and is compatible with the basic VectorStar ME7838 system. Dynamic range of the VectorStar ME7838D broadband system is 120 dB at 10 MHz, 110 dB at 67 GHz, 109 dB at 110 GHz and 94 dB at 145 GHz. Stability is 0.1 dB over 24 hours; throughput is further improved by the instrument's measurement speed of 110 msec for 401 points at 10 kHz IFBW.

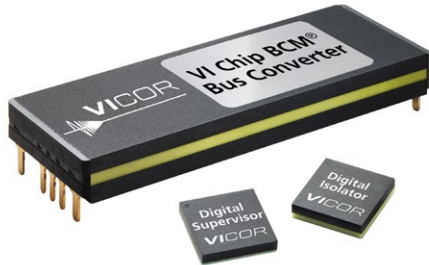


Complete article, here



DC/DC converters surpass 2.5 kW/in³

Vicor has further increased power density, and added digital communication capability, with products added to its ChiP Bus Converter Module (BCM) product family: these ChiP-based BCMs provide power density of 2750 W/in³, supplying up to



1.75 kW with 98% peak efficiency. Vicor has also introduced digital telemetry and control capabilities for its ChiP BCM portfolio, available as an option for the new 1.75 kW modules and previously announced 1.2 kW modules. A PMBus compliant digital interface option gives system designers access to the ChiP BCM's internal controller, enabling digital communication with an array of ChiP BCMs via a single bus for control, configuration, monitoring and other telemetry functions. The 1.75 kW modules support a nominal input voltage of 400V and nominal output voltage of 50V, with a K-factor (fixed conversion ratio) of 1/8.

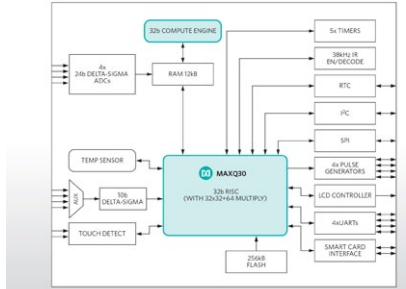
Complete article, here

High-integration, single-phase metering SoC

Maxim Integrated's ZON M3 single-phase energy meter SoC enables $\pm 0.1\%$ accuracy over a 5000:1 dynamic range. Designed as a highly accurate, low-cost design system for e-meters and solid-state meters, the ZON M3 energy-meter solution integrates four 24-bit ADCs for 4-channel data collection and $\pm 0.1\%$ measurement accuracy over 5000:1 dynamic range.

A 32-bit metrology compute engine (CE) ensures high-accuracy processing of all collected data. Its two touch-switch inputs eliminate mechanical switches, and its infrared (IR) communications interface

ZON M3: Maxim Integrated's Single-Phase Electricity Meter SoC



eliminates the typical extra IR receiver module. All the high integration reduces cost and improves user experience. The device offers metering accuracy of over $\pm 0.1\%$ over 5000:1 dynamic range, and high integration with touch-switch inputs, IR communications and multiple interfaces (SPI, I²C, and 4 USART). In a 100-pin LQFP package, the ZON M3 electricity meter costs \$2.81 (1000).

Complete article, here

GPS modules for wearables boost location performance

CSR and OriginGPS (Israel) have announced high-performance GNSS modules using CSR's SiRFstarIV and SiRFstarV product lines. The new modules are 70% smaller than

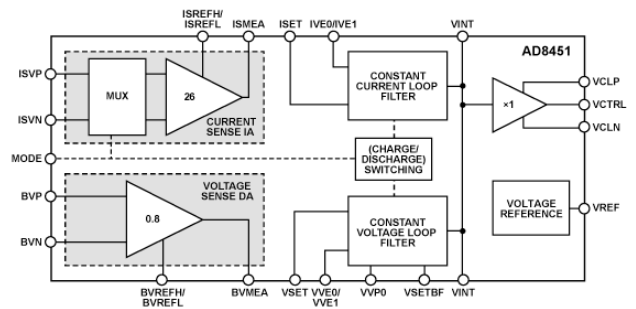
current solutions and deliver a 30% reduction in Time To First Fix (TTFF), making them suitable for health and fitness trackers, sports watches, medical devices, wearable action cameras, and digital still cameras. All modules, including the 7 x 7mm Multi Spider (ORG4572) solution, integrate the LNA, SAW filter, TCXO, RTC crystal and RF shield.

The OriginGPS modules offer high sensitivity resulting in shorter autonomous and aided TTFF, better navigation stability, and higher accuracy in harsh environmental conditions. In real-life testing of the module in camera applications, TTFF performance improves by over 30% compared to other solutions. The module also delivers TTFF results in less than one minute over 90% of the time (Cold Starts).

Complete article, here

Precision battery monitor and controller

Analog Devices' AD8451 is a precision analogue front end and controller for testing and monitoring battery cells. A precision fixed gain instrumentation amplifier (IA) measures the battery charge/discharge current, and a fixed gain difference amplifier (DA) measures the battery voltage. Internal laser



trimmed resistor networks set the gains for the IA and the DA, optimising the performance of the AD8451 over the rated temperature range. The IA gain is 26 and the DA gain is 0.8. Voltages at the I_{SET} and V_{SET} inputs set the desired constant current (CC) and constant voltage (CV) values. CC to CV switching is automatic and transparent to the system. A TTL logic level input, MODE, selects the charge or discharge mode (high for charge, low for discharge). An analogue output, VCTRL, interfaces directly with Analog Devices' ADP1972 PWM controller.

Complete article, here

Power module with ultra-wide voltage input

A 50W ultra-wide-input power module in sixteenth-brick footprint simplifies Power-over-Ethernet (PoE) applications; ultra-wide input voltage from 18V to 75V accommodates 24V and 48V systems, reduces inventories and is also suitable for remote power feed applications. The module is the latest evolution of Ericsson's PKU family and combines the thermal enhancements integrated in

the recently announced PKU4116C module together with an optimised fly-forward topology. The PKU5510E delivers an output current of 15A at 3.3V output and has a built-in functional isolation of 2250Vdc that meets the requirements specified by the IEEE802.3 Ethernet networking standard, and also meets Basic Insulation requirements according to IEC/EN/UL60950. The PKU5510E has been designed for applications that have to accommodate both telecom system bus voltages of 24V and 48V, and also able to supply voltages to Power-over-Ethernet based applications.



[Complete article, here](#)

Current transducers measure to 25A, in PCB-mount format

LEM has added to its range a series of open-loop Hall-effect ASIC based devices measuring up to 25A DC, AC or pulsed; with over-current detection and fault reporting functions, they operate over -40 to +105°C and have a PCB-mount design with aperture for the primary conductor. In the HO series of PCB-through-hole mounting current transducers, these units provide an aperture of 8 x 8 mm to carry the primary conductor under measurement, extending the options for this form-factor.

The new models, for 6, 10 or 25 A nominal measurements of DC, AC, and pulsed signals use LEM's latest Open-loop Hall-effect ASIC introduced with the launch of the HO 8, 15 and 25-NP & -NSM models. A high level of insulation between primary and measurement circuits, due to the high clearance and creepage distances of more than 8mm and a CTI (comparative tracking index) of 600, allows a test isolation voltage of 4.3 kVRMS/50 Hz/1 min.



[Complete article, here](#)

Bluetooth LE protocol gains over-the-air upgrade

Ultra low power (ULP) RF specialist Nordic Semiconductor has announced S110 SoftDevice v7.0, a major release of its Bluetooth low energy stack, for the nRF51822 Bluetooth low energy and 2.4GHz proprietary System-on-Chip (SoC) and the nRF51422 ANT and ANT/Bluetooth low energy multiprotocol SoCs. (A SoftDevice is Nordic's self-contained stack for nRF51 Series SoCs that incorporates an RF protocol and its associated management framework.) S110 SoftDevice

v7.0 brings a range of features including Over-The-Air Device Firmware Upgrade (OTA-DFU), concurrent Peripheral / Broadcaster roles, support for concurrent multiprotocol Bluetooth low energy/2.4 GHz RF proprietary operation, and compliance with the latest version of Bluetooth wireless technology (Bluetooth v4.1) allowing end products using the S110 SoftDevice to be qualified to the Bluetooth standard.

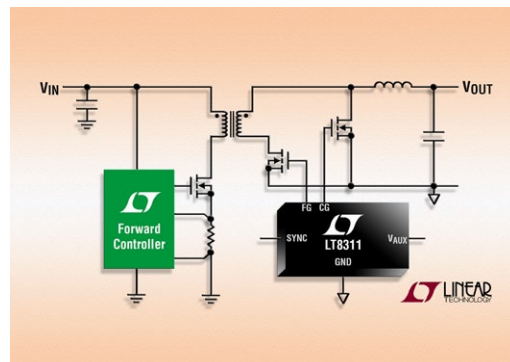


[Complete article, here](#)

Transformer-less synchronous MOSFET driver

LT8311 is a high efficiency secondary-side MOSFET driver that operates without the need for primary control in an isolated synchronous forward converter. The LT8311's preactive mode eliminates the need for a signal transformer for primary to secondary-side communication by sensing signals on the secondary side to control synchronous rectification.

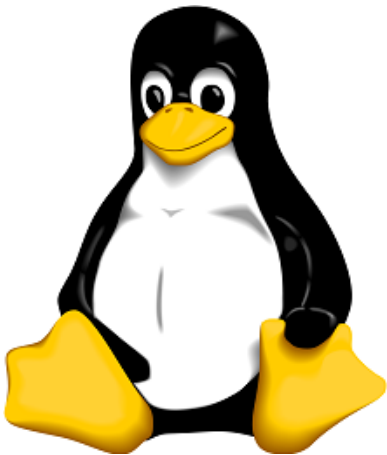
This mode reduces component count and solution size. The device operates over a 3.7V to 30V input voltage range and is used with a primary-side IC, such as the LT3752/-1. The complete forward converter can operate with input voltages ranging from 6.5V up to 400V+ making it ideal for a wide range of applications including hybrid/electric vehicle automotive requirements. It combines a 10 mA opto-driver and a feedback loop error amplifier to enable output voltage feedback from the secondary to the primary side. The entire system provides fixed frequency peak current mode control.



[Complete article, here](#)

TI Sitara MCUs based on Mainline Linux kernel

Basing its kit around, Texas Instruments says, a high-quality, stable Linux platform, the Mainline Linux kernel support enables ease of migration by providing consistent access to new devices and the latest features. TI's Sitara Linux SDK provides a robust, stable Mainline Linux kernel for developers using TI's Sitara processors. To ensure high quality, TI collaborates with the Kernel.org community for code reviews with stringent acceptance criteria. TI also continuously stress tests the Linux kernel across various customer use cases and applications to guarantee stability. TI's Sitara Linux SDK 7.0, supporting the latest Mainline Linux kernel, is available to download today, along with a range of supporting information. The SDK is currently compatible with Sitara AM335x processors. Future TI devices with Linux software support will include TI's Sitara AM4x and AM5x processors as well as TI's KeyStone multicore system-on-chips based on ARM cores.



Complete article, here



ARM-based Kinetis MCUs for motor control

Freescale Semiconductor's lead families of the new Kinetis V series, based on ARM Cortex-M cores, are optimised for motor control and digital power conversion applications. Freescale accompanies them with the Kinetis Motor Suite tool. The KV4x family is the flagship of the existing V series, targeting digital power conversion designs, as well as PMSM and ACIM applications requiring high dynamic control. KV4x MCUs incorporate a 150 MHz ARM Cortex-M4 processor with floating-point unit executing from up to 256 kB of Flash memory via a 128-bit wide interface that minimises CPU wait states. With up to 30 timer channels – twelve provided by the flexible eFlexPWM – KV4x family devices provide multiple three-phase motor drive capabilities supporting dead time insertion, complementary pairing of PWMs, half cycle reload and fault detection. For sensorless motor control speed/position detection, two 12-bit ADCs support sample rates of up to 1.9 Msamples/sec and can be triggered by any module connected to the MCU's internal peripheral crossbar, including timers, analogue comparators or GPIO. For switched mode power supply applications, an eFlexPWM module provides 300 picosecond resolution, while the ADCs sample at 4.1 Msamples/sec. This improves real-time control, ensuring that critical timing windows for data gathering and system updates are met.

Complete article, here



Extended temperature range for ARM MCUs

For extreme industrial environments, NXP Semiconductors has added LPC microcontrollers rated for temperatures up to 105°C. The LPC11E6x family is designed for harsh operating conditions common in many industrial, lighting, and industrial automation applications. The LPC11E6x family is available in three memory and package variations, including up to 256 kB Flash, 36 kB RAM and 4 kB EEPROM. Power efficiency is achieved through an ARM Cortex-M0+ core and NXP's power profiles that allow various power saving options depending on the application demands. High-precision analogue features include a 2 Msamples/sec, 12-channel, 12-bit ADC, and connectivity is provided through I²C and SPI interfaces, USARTs, and up to 80 GPIOs. Also new to the LPC1100 Series, the LPC11E6x's two on-chip SCTimer/PWMs support advanced timing features. This block can be configured as multiple PWMs, a PWM with dead-time control, a PWM with reset capability, and many other functions.



Complete article, here



Highly-integrated WiFi in 14 x 16 mm

Econais has what it claims is the smallest, most integrated Wi-Fi (SiP) module; the integrated hardware/software and low standby power requirements simplify smart home, M2M and IoT device design and development. EC19W01 is an 802.11b/g/n Wi-Fi System In Package (SiP) module that has low power drain and features fully integrated MCU, Wi-Fi, cloud connectivity, flash and antenna that is fully certified FCC, EC, IC, and TELEC. The module incorporates Wi-Fi 802.11b/g/n standards and is fully certified with FCC, EC, IC, and (soon) TELEC. Features include AirPlay, Wi-Fi Direct, ProbMe configuration, full TCP/IP stack, HTTPS/SSL, DHCP Client/Server, WPS, legacy Wi-Fi Client and SoftAP modes with WPA/WPA2 support, Serial to Wi-Fi, and Cloud Service Support; the EC19W01 is 14x16x2.8mm in size.



Complete article, here



It's the firmware, of course

Have you ever had to troubleshoot a design you didn't know much about? Anyone who is working around complex systems today will likely be faced with such a task, especially if that person has a reputation as the troubleshooter. I've sometimes made the mistake of cultivating such a reputation.

A product landed in my lap one day, and it was a tiny bit flaky. Every so often on power-up – maybe 5% of the time – it would just sit there, stare back at me, and refuse to do anything. This was pricey consumer gear, and our customers would not be amused.

Fortunately, I was already familiar with the general design of the box, an AV media server. I laid out the guts on my lab bench and started playing. I discovered that, when the box appeared to be dead in the water, it was actually mostly functional. Only the front panel was hung up.

This box had a small PC motherboard in it, and the motherboard connected to the front panel via an internal USB connection. The USB wasn't called on to do much, though – just handle some lights and buttons.

I can't remember the exact chain of events, but I somehow quickly decided that the problem lay with this USB connection. The trouble was that I knew next to nothing about USB: two data/two power, bit rates, and something about pullup resistors. After hitting the Web for 20 minutes, I felt suitably prepared to attack the problem – with the aid of my scope, of course.

I clipped probes onto the data-in and -out lines and started hitting that power button. I could see bursts of activity on the USB link – always the same – unless the front panel decided to hang up. When that happened, I would see initialization data coming in vain from the PC. The microcontroller on the front panel would not respond.

Continuing to play with this setup, I found that the failures only happened within a certain band of off-times. If the power was turned off for a short period

and then back on, the system would come back up smiling. Ditto if it had been off for a long period. Very interesting.

After verifying there was nothing obviously wrong with the hardware, I let my mind wander a bit. What about the microcontroller firmware? I thought back to my early computer days, and how processors and memory would remember data for a while, even after their supply voltage had dropped to zero. Or how memories would generally power up with a default data pattern – not 100% reliably of course, but not randomly either.

I thought, "What if there's a wee bug in the firmware? Could a certain memory startup pattern cause the failures we're seeing?" The more I played, the more I was convinced that the misbehaviour was due to some sort of microcontroller initialisation problem.

I left the reassuring glow of my scope and tracked down the person who had

written the code. "I think there's some sort of initialisation bug in your startup code," I told him.

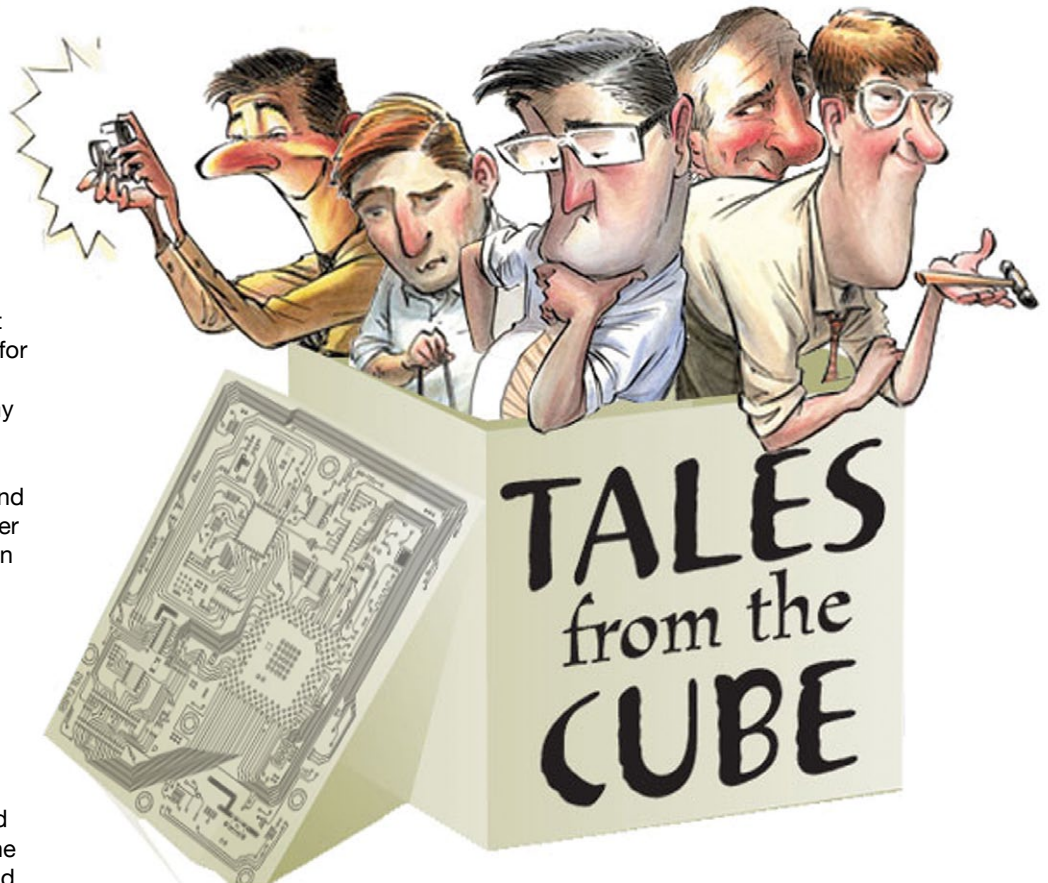
He looked unimpressed.

"Let's go look at your code. I want to see what it's doing," I said.

He looked unconvinced.

I finally dragged him back to his desk and we started scanning the code. It was in assembler, which I tend to enjoy, but it wasn't an instruction set I was overly familiar with. He started mentally stepping through the reset code, and within 30 seconds, he looked at me and pointed to the problem. Some memory was not being initialised, and some wrong addresses were.

The memory of my victory over the miscreant firmware has become fuzzy with age. I mostly just remember my triumph of reasoning. But I was very humble, of course. It was just a guess, after all. OK, maybe I wasn't so humble.



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